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(54) Title: SYSTEM AND METHOD FOR TESTING INTEGRATED CIRCUIT DEVICES

(57) **Abstract:** The invention disclosed herein is a system and method for testing integrated circuit devices, including memory chips. The devices under test are subject to behavioural testing, in which a copy of signals in an application system is directed to the device under test, or to an electronic component connected to the device under test. This permits the device under test to be tested under the operating conditions of the application system, which is preferably similar to the actual application environment in which the device under test will ultimately be used. Conventional tests, including pattern testing and/or parametric tests, may also be performed on devices under test, if desired.

Title: SYSTEM AND METHOD FOR TESTING INTEGRATED CIRCUIT DEVICES

FIELD OF THE INVENTION

This invention relates to a system and method for testing integrated circuit devices. More specifically, this invention relates to a system and method that permits integrated circuit devices to be tested in an environment which is representative of the application environment (e.g. a personal computer or PC) in which the integrated circuit device will be used.

BACKGROUND OF THE INVENTION

Typically, integrated circuit devices are subject to rigorous testing before they are sold or put to their intended use. For example, each integrated circuit device is tested to determine whether or not it meets the specifications for that type of device as determined by the manufacturer.

One example of an integrated circuit device which is commonly tested prior to its use in commercial applications, is a memory chip. Not only are memory chips subject to testing to determine whether they meet the specifications for those types of chips as specified by the manufacturer, but the memory chips are also typically subjected to other conventional tests such as pattern testing and parametric tests. Memory chip pattern testing is an organized method of exercising each memory cell in a memory chip to verify its functionality. Parametric tests verify component operating parameters such as power consumption, standby current, leakage current, voltage levels and access time.

Conventional tests are used to verify component functionality in an attempt to reveal whether or not the chip being tested is likely to fail under its intended use. While most conventional tests performed on memory chips are successful to varying degrees at detecting, for example, parametric failures, hard failures (e.g. a memory cell stuck at 1 or 0), soft failures (e.g. crosstalk or linkage between memory cells), and refresh failures, conventional testing systems and methods do not readily detect

behavioural failures. A behavioural failure is one that will occur when the memory chip is used in an actual application system (for example, a failure that results as a result of the execution of a specific command or access sequence found in normal PC operations). It is very difficult for conventional testing systems and methods to detect such failures, since the tests employed are not truly indicative of how a memory chip will behave under its intended application. In fact, a memory chip that has only been subject to conventional tests will have never been operated in an actual application environment.

Systems and methods for testing integrated circuit devices, and particularly for integrated circuit memory devices, are well known in the prior art. For example, U.S. Patent No. 5,794,175 discloses test equipment for semiconductor devices that allow for the testing of large arrays of semiconductor memory chips in parallel. Test patterns are generated and subsequently written to and read from the memory chips. A comparison is made between the expected values and the actual values of data read from the memory chips to determine if the memory chips are faulty.

U.S. Patent No. 5,959,914 discloses an apparatus including a controller which can transfer test data to and from memory devices. The controller can generate data patterns which are written to the memory devices, and can read the data back from those memory devices. The data read back from those memory devices is then compared to the data which was written to those memory devices, and information relating to errors as indicated by discrepancies between the two sets of data can be stored or outputted.

U.S. Patent No. 4,965,799 discloses a method and apparatus for testing the functionality and maximum operating speed of a DRAM chip. In this method, data bit patterns are generated and written into the memory cells of a memory device. The patterns stored and subsequently read are compared with the patterns initially generated, and if there are any differences between the read patterns and the generated patterns, an appropriate indication is provided, by a series of light-emitting diodes

(LEDs) for example.

U.S. Patent No. 4,379,259 discloses a process and system for simultaneously testing numerous integrated circuit memory chips. More specifically, the patent relates to a method wherein a number of individual memory chips are mounted on one of a number of memory boards, and subsequently each board is connected to a PC driver card. Pattern testing, and testing to the specifications of the chips are performed on the memory chips.

While these prior art systems and methods for testing integrated circuit devices may be effective in detecting many of the common failures that can be revealed by pattern testing and tests against device specifications, these conventional testing systems and methods will not be as effective in detecting behavioural failures as the testing environment is likely to be dissimilar from the actual application environment in which the particular device being tested will ultimately be used. For example, the device under test may pass all conventional tests but may fail under "real world" operating conditions (e.g. during a Windows® setup).

One possible method of performing behavioural testing on, for example, a memory chip, is to directly use the memory chip in an application system (e.g. a PC). However, directly incorporating the memory chip under test in an application system to perform a behavioural test in this manner has numerous drawbacks. First, the memory chip under test would generally be required to store the testing program itself or a part thereof, thus hindering efficient testing of the entire memory space of the memory chip. Second, a faulty memory chip under test may cause the entire application system to crash, preventing further testing of the memory chip, and requiring the system to be restarted prior to testing the next memory chip. This is an inefficient testing method if numerous memory chips are to be tested. Third, it is difficult to perform behavioural testing on multiple memory devices simultaneously with one application system in this manner. Fourth, the sequence of operations that would be performed on a memory chip under test during the execution of a test program will not be

truly representative of the sequence of operations that would be performed on a memory chip used in a PC under "real world" operating conditions. Fifth, testing a memory chip directly in an application system will not usually provide for the flexibility of also allowing critical and standard parameters for memory (e.g. setup time, hold time, V_{OL}, V_{OH}, etc.) to be altered while operating in a test mode.

Accordingly, there is a need for a system and method for testing integrated circuit devices in an environment which is representative of the actual application environment in which the integrated circuit device will ultimately be used.

Further, there is a need for a system and method for testing an integrated circuit device that can test the ability of a device to operate within the range of the specifications for that device and also under conditions that would arise when used in its intended application environment.

Still further, there is a need for a system and method for testing integrated circuit devices, including memory chips for example, that more effectively tests the devices for failures by combining conventional tests methods (e.g. pattern testing) and behavioural testing in a single process.

SUMMARY OF THE INVENTION

The invention is a system and method for testing integrated circuit devices, including memory chips. Devices under test are subject to behavioural tests, in which a copy of signals in an application system are directed to the device under test, or to an electronic component connected to the device under test. This permits a device to be tested under the same operating conditions as the actual application environment in which the device will ultimately be used.

More specifically, the invention provides for a method for testing an integrated circuit device where signals transmitted to a device in an application system are also transmitted to a device under test, the responses of these two devices to the signals are determined, and the responses subsequently compared.

The invention also provides for a method for testing an integrated circuit device where signals transmitted to a first controller connected to a device in an application system are also transmitted to a second controller connected to a device under test, the responses of these two controllers to the signals are determined, and the responses subsequently compared.

The invention also provides for a system for and method of testing an integrated circuit device in which the device under test is subject to both conventional tests and behavioural testing.

The invention also provides for a system for testing an integrated circuit device comprising a device under test; a device operating in an application system and system connections connecting the device to other components in the application system; a set of test components connected to the device under test, where the set of test components are adapted to direct a copy of the signals carried by the system connections to the device under test; and a comparator adapted to compare the responses to the signals by the device under test and the device in the application system.

The invention also provides for a system for testing an integrated circuit device comprising a device under test connected to a test controller; a device operating in an application system connected to a system controller; system connections connecting the system controller to other components in the application system capable of providing input to the system controller; test components adapted to direct a copy of the signals carried by the system connections to the test controller; and a comparator adapted to compare the responses by the test controller and system controller to the signals.

BRIEF DESCRIPTION OF THE DRAWINGS

For a better understanding of the present invention, and to show more clearly how it may be carried into effect, reference will now be made to the accompanying drawings, wherein:

Figure 1 is a schematic diagram illustrating a typical conventional testing system for integrated circuit memory devices;

Figure 2A is a schematic diagram illustrating some components of a memory application system;

Figure 2B is a schematic diagram illustrating the basic architecture of a behavioural testing system;

Figure 2C is a schematic diagram illustrating some of the components of a typical PC application system;

Figure 3 is a schematic diagram illustrating a preferred embodiment of the present invention;

Figure 4A is a schematic diagram illustrating another preferred embodiment of the present invention;

Figure 4B is a schematic diagram illustrating the embodiment of Figure 4A implemented using two circuit boards;

Figure 5 is a schematic diagram illustrating another preferred embodiment of the present invention;

Figure 6 is a flowchart illustrating the steps performed in a method of testing memory chips;

Figures 7A and 7B are flowcharts illustrating the steps in alternate embodiments of a method in which memory chips are subject to behavioural testing;

Figure 8 illustrates an arrangement and apparatus for tapping a memory bus in a variant embodiment of the invention;

Figure 9 is a schematic diagram illustrating an embodiment of the invention in which a parametric control device is used;

Figure 10 is a schematic diagram illustrating a variant embodiment of the invention in which multiple devices under test are tested in parallel; and

Figures 11A, 11B, 11C and 11D are schematic diagrams illustrating variant embodiments of the invention in which application signals being supplied to testing components are stored in a memory device.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

For clarity, before discussing the present invention in detail, a brief discussion of aspects of typical conventional memory device testing systems and application systems will be provided with reference to Figures 1 and 2a.

Referring to Figure 1, a typical prior art conventional testing system for integrated circuit memory devices is shown generally as 10. The system 10 includes a test pattern generator 12 which is capable of generating test patterns to be used in testing the storage elements of a memory "device under test" 14, hereinafter referred to as a DUT. The test pattern generator 12 may be connected to a set of one or more drivers and/or logic devices 16 by way of, for example, address lines, data lines, and/or control lines. The test pattern generator 12 provides output by way of signals carried by the lines connecting the test pattern generator 12 to the set of one or more drivers and/or logic devices 16.

For example, the output of the test pattern generator 12 may correspond to instructions for performing the following operations on a DUT 14:

Sample test algorithm:

1) From the first to last memory address, write "0";
2) From the first to last memory address, read "0", write "1";
3) From the first to last memory address, read "1", write "0";
4) From the first to last memory address, read "0".

The set of one or more drivers and/or logic devices 16 converts the output provided by the test pattern generator 12 into a set of signals compatible with the specific DUT 14. For example, a first logic device may be required to translate a linear memory address number provided by the test pattern generator 12 into a format consistent with the addressing method of the DUT 14 (e.g. translating an address identifier to a corresponding series of bank, row, and column identifiers). A second logic

device may also be required to format the addressing parameters (e.g. represented as bank, row, and column identifiers) into an address identifier that can be carried by a series of address lines connected to the DUT 14, and that can be understood by the DUT 14. Essentially, the purpose of the first and second logic devices is to translate the information from the test pattern generator 12 into a series of commands that can be understood by the specific DUT 14. The output from these logic devices may then be directed to a driver which provides an interface to the DUT 14, and which directs signals corresponding to the instructions provided by the test pattern generator 12 to the DUT 14. The driver can be programmed to provide signals to the DUT 14 while varying specified operating parameters (e.g. signal magnitude, V_{OL}, V_{OH}, rise time, fall time, hold time, setup time, etc.).

In summary, the set of drivers and/or logic devices 16 function to apply the test patterns generated by the test pattern generator 12 to the DUT 14 in a format compatible with the DUT 14.

In response to a "read" instruction generated by test pattern generator 12, data is read from the DUT 14 and subsequently outputted to a data receiver 18. A comparator 20 compares the expected data to be read as provided by the test pattern generator 12 with the data read from the DUT 14 as stored in the data receiver 18.

It will be obvious to those skilled in the art that the comparator 20 may be programmed or designed to accommodate the delay resulting from the passing of instructions of the test pattern generator 12 through the set of drivers and/or logic devices 16, the DUT 14 and the data receiver 18 to the comparator 20. Alternatively, other electronic components may be inserted between the test pattern generator 12 and the comparator 20 to ensure that the data provided by the pattern generator 12 and the data stored in the data receiver 18 being compared are synchronized.

The results of the comparison of the data from the test pattern generator 12 and the data receiver 18 as determined by the comparator 20 is outputted to an output module 21. The output module 21 can redirect the results of the comparison to an error logging unit 22 which may store a

record of any errors found. The output module 21 may also redirect the results of the comparison to a display 23 (e.g. providing information on errors on a visual display, or through a set of light-emitting diodes) or other output device. An error will be detected if the data stored in the data receiver 18 does not correspond to the expected data as indicated by the test pattern generator 12.

Referring to Figure 2A, some components of a typical memory application system 25 are shown. In Figure 2A, the typical memory application system 25 comprises application system components 26 which include a memory controller, connected to a target memory device 27 (i.e. system memory) by bus A 28, bus B 29, and bus C 30. Bus A 28 represents a unidirectional signal bus (one or more parallel wires) used to transfer signals from the application system components 26 which include a memory controller, to the target memory device 27. Bus B 29 represents a bidirectional signal bus (one or more parallel wires) used to transfer signals from the application system components 26 which include a memory controller, to the target memory device 27, and to transfer signals from the target memory device 27 to the application system components 26 which include a memory controller. Bus C 30 represents a unidirectional signal bus (one or more parallel wires) used to transfer signals from the target memory device 27 to the application system components 26 which include a memory controller. During the course of a normal operation of the typical memory application system 25, signals are transmitted from the application system components 26 which include a memory controller, to the target memory device 27 using bus A 28 and bus B 29 (e.g. when writing data to the memory device), and signals are transmitted from the target memory device 27 to the application system components 26 which include a memory controller, using bus B 29 and bus C 30 (e.g. when reading data from the memory device).

In the specification and the claims, an application is the system, product, equipment or device that can use the component being tested. If the component to be tested is a memory chip, the application

could be a computer, an appliance, a video card for a PC, a digital TV, an MP3 player, a camera, a voice recorder, a subassembly, a server, networking equipment, a cell phone, an information appliance, or any other electronic product using memory chips. An application system is the hardware and software that comprise the application, and may be "off-the-shelf" or custom-designed. A component may be a single integrated circuit chip or a group of integrated circuits on an assembly or printed circuit board, for example. Further, components can be bare silicon die, assembled die, packaged integrated circuits, stacked integrated circuits, or any of these connected together, for example.

It is a requirement of the present invention that behavioural tests be performed on an integrated circuit device under test, which may be for example, a memory device in a memory application system. Generally, when behavioural tests are applied to a device under test, the device under test is subject to the same system interactions as the device under test may be exposed to when it is eventually used in its intended application environment.

For example, behavioural tests can attempt to detect application-specific failures. An application-specific failure occurs when an application does not function as expected only under certain conditions relating to, for example, the application environment (i.e. conditions of the system, product, equipment or device that affect the electrical operations of the application, including for example, temperature, humidity, signal level and strength, electromagnetic interference, crosstalk, plus ground, background, and signal noise), or the operation of the application with specific types of hardware or software. For example, if a component causes an application system such as a PC to fail only during the installation of a given software program or the operation of a given brand of peripheral hardware device (e.g. a specific brand of video card), this could be categorized as an application-specific failure.

As a further example, behavioural tests can attempt to detect access behavioural failures. Every application system has its own method

of accessing its components (e.g. memory chips). The combination of operating hardware and software comprising an application system can create a unique access sequence to its components. If the component cannot operate as intended under this unique access sequence, this is categorized as an access behavioural failure. Thus, a component could suffer from an access behavioural failure even if it had passed all conventional tests. For example, if a memory chip passes conventional tests but fails only when a PC continuously writes the same data to the same memory address during a CPU handling interrupt, this could be categorized as an access behavioural failure.

Referring now to Figure 2B, shown therein is a basic configuration of a behavioural testing system made in accordance with the present invention. In Figure 2B, buses 28, 29, 30 are tapped using tapping connections 31 to redirect a copy of the signals on the buses 28, 29, 30 to a number of testing components 32. The testing components 32 communicate with the device under test 33 through connecting buses 34, 35, 36. The set of connecting buses 34, 35, 36 transfer data to and from the device under test 33 in the same manner as buses 28, 29, 30 transfer data to and from the target memory device 27 respectively.

The testing components 32 are adapted to direct a copy of signals being received by the target memory device 27 over buses 28, 29 to the device under test 33 using buses 34 and 35. Accordingly, when data is being written to the target memory device 27, the data will also be written to the device under test 33.

When the target memory device 27 receives a read instruction, the target memory device 27 will output data to the memory controller by transmitting signals over buses 30 and/or 29. A copy of these outputs can be directed to the testing components 32 through tapping connections 31.

Since the device under test 33 will receive the same read instruction as the target memory device 27 (as the testing components 32 are adapted to provide the device under test 33 with the same signals being provided to the target memory device 27), the device under test 33 will also

consequently output data by transmitting signals over buses 36 and/or 35, connected to the testing components 32.

The outputs from the target memory device 27 over buses 29 and 30, and the outputs from the device under test 33 over buses 35 and 36 are received by the testing components 32. Testing components 32 may comprise an error logging unit 37, which may be, for example, a logic device that compares the outputs from the target memory device 27 and the device under test 33 (e.g. using a series of exclusive-or gates), and outputs the results of the comparison. Thus, if the device under test 33 operates in the same manner as the target memory device 27, the output from the respective devices should be the same. If the outputs differ, then an error will be detected by the error logging unit. Preferably, the target memory device 27 is a "good" chip which has been previously tested as being suitable for this application, since the functionality of the device under test 33 is being compared to that of the target memory device 27. In this manner, the target memory device 27 acts as a reference device.

The testing components 32 will also comprise connections, transceivers, and other logic devices and/or electronic components (e.g. a command decoder, a bidirectional input buffer used to temporarily latch the bidirectional bus and to give time for the command decoder to determine the direction of the signals on that bus and to redirect the signals to the device under test or the error logging unit accordingly) to facilitate the redirection of signals to the target memory device 27 on buses 28, 29, 30 of the application system 25 to the device under test 33, to read the output signals from the target memory device 27 and the device under test 33, and to compare those signals.

Referring now to Figure 2C, a typical system architecture for a personal computer (PC) is shown generally as 38. This is one example of a memory application system for which a memory device may be tested if this is a type of system in which the memory device under test can actually operate in.

The memory application system 38, in this typical

configuration, comprises a processor chip 40 connected to a memory controller/graphics controller hub 42 (hereinafter referred to as "system memory controller") by a system bus 44. The system memory controller 42 comprises one or more controller chips that control various connected devices, including system memory 46 through a memory bus 48. The memory bus 48 will typically comprise multiple sets of parallel wires, some of which only carry signals being transmitted to system memory 46 (as in Bus A 28 of Figures 2A and 2B), some of which only carry signals being transmitted from system memory 46 (as in Bus C 30 of Figures 2A and 2B), and some of which carry signals that may be transmitted in both directions (as in Bus B 29 of Figures 2A and 2B). The memory application system 38 may also comprise controller chips that control one or more video controllers or devices 50 through one or more video device connections 52a, 52b (e.g. an AGP graphics controller connected to the memory controller/graphics controller hub 42 by an AGP bus). A video device connection may be unidirectional (e.g. video device connection 52a) or bidirectional (e.g. video device connection 52b).

The system memory controller 42 is also connected to an I/O controller hub 54 by a hub interface 56. The I/O controller hub 54 comprises one or more controller chips for communicating with one or more peripheral device controllers or peripheral devices 58 through one or more I/O connections 60. An I/O connection 60 may be unidirectional or bidirectional.

Each of the video device connections 52a, 52b, and I/O connections 60 may comprise a single wire, a set of parallel wires (e.g. a bus), or electronic components permitting wireless communications between the controller hubs 42, 54 and connecting devices 50, 58 as is known.

The system memory controller 42 and connected I/O controller hub 54 may be commercially available as a package 62 (e.g. Intel® 815 chipset).

Figures 3 through 5 illustrate several preferred embodiments of a behavioural testing system made in accordance with the present

invention that can be used in testing a memory device of the same type as that being used as system memory 46 in an actual operating PC. As noted above, a PC is one example of a memory application system 38 to which the present invention may be applied. Advantageously, the memory device under test will be exposed to the interactions between system memory 46 and other components of the memory application system 38 in a minimally obtrusive manner (e.g. by not directly replacing system memory 46 with the memory device under test), while the memory device under test is operated in a manner that is extremely close to the environment in which it will eventually be used (i.e. using a similar application system). This can be performed by combining an add-on test device (which is more specifically, a combination of hardware components, circuitry and software) to an application system to obtain a behavioural testing system.

A behavioural testing system can comprises hardware (equipment, one or more electronic devices, circuitry, etc.) and software, and is designed to analyze one or more devices under test. Advantageously, the behavioural testing system is designed so that the application system is still fully functional even when the device under test is not present in the behavioural testing system, and so that the functions of the application system are not affected by either the quality of the device under test or the test results. For instance, a PC (or motherboard) cannot, on its own, function as a behavioural testing system for memory modules because the memory module under test must be installed for the PC to operate, and because a defective module could cause the PC to malfunction. Furthermore, preferably, a defective device under test will not cause the behavioural testing system to malfunction; instead, the behavioural testing system is adapted to detect and indicate the cause of failure.

Referring now to Figure 3, a preferred embodiment of a behavioural testing system representing a basic implementation of the present invention is shown generally as 118. Behavioral testing system 118 is constructed by building upon a memory application system 38 (e.g. as in Figure 2c) so as to provide copies of signals being carried by connections in

the memory application system 38 to testing components 119 of the behavioural testing system 118. The testing components 119 may be pre-combined into a single add-on test device to be connected to the memory application system 38.

In this embodiment of the invention, the memory bus 48 connecting the system memory controller 42 and system memory 46 is directly tapped. A tapping connection 120 is made to the memory bus 48 at 121, and preferably the tapping connection 120 has the same number of wires as the number of active wires that comprise the memory bus 48 (i.e. wires of the memory bus which are not used by system memory 46 or which do not affect the operation of system memory 46 may be ignored) so that, in essence, the signals carried by the memory bus 48 will be reproduced on the tapping connection 120. Tapping connection 120 is also connected to one or more transceivers 122. The transceivers 122, being compatible with the signal levels of the signals carried by the memory bus 48 being tapped, strengthen the signals carried by tapping connection 120, and retransmit these signals to a control logic device 123 through intermediate connection 124. Preferably, transceivers 122 have a high input impedance so that degradation of the signals being carried by the memory bus 48 is minimized. Advantageously, the transceivers 122 are unidirectional and prevent signals from the testing components 119 from interfering with the communication between components of the memory application system 38.

When the system memory controller 42 attempts to write data into system memory 46, the control logic device 123 directs a copy of the signals carried by memory bus 48 corresponding to the write operation, to a driver 124 which causes the same data to be written to the memory device under test (DUT) 125. Similarly, when the system memory controller 42 attempts to read data from system memory 46, signals corresponding to the read operation are also directed through the driver 124 to the DUT 125. Subsequently, the read data from the DUT 125 is outputted to a data receiver 136. The data read from system memory 46 carried by the memory bus 48 is also directed to the control logic device 123, and a comparator

138 connected to both the control logic device 123 and the data receiver 136 determines if there are any differences in the two sets of data read from the two memory devices, namely the system memory 46 and the DUT 125.

The system memory 46 acts as a reference device, since it is used to provide the expected data or result in comparisons with the data or results obtained from the DUT 125. Therefore, the system memory 46 is preferably a known "good", fully qualified device that is either the same type as the DUT 125, or is functionally equivalent to the DUT 125.

The results of the comparison as determined by comparator 138 can be outputted to a microcontroller 139, which can direct the output to the memory application system 38 itself through connection 140, or to another output device, an error logging unit, a separate application system, a microprocessor, a display, a set of light-emitting diodes (LEDs), one or more error indicators (e.g. visual indicators, aural indicators, a combination of these), or an electronic component connected to one or more of these elements, for example.

Referring to Figure 4A, another preferred embodiment of the behavioural testing system of the present invention is shown generally as 168. Behavioural testing system 168 is also constructed by building upon an existing memory application system 38 so as to provide one or more copies of signals being carried by one or more application system connections (e.g. 44, 52b, 56) to testing components 169 of the behavioural testing system 168 as described below. The testing components 169 may be pre-combined into a single add-on test device to be connected to the memory application system 38. As previously noted, each system connection in the memory application system 38 may be unidirectional or bidirectional, and each system connection may comprise a single wire, a set of parallel wires, or electronic components permitting wireless communication between connected devices.

More specifically, the behavioural testing system 168 is initially constructed by providing a means for retrieving a copy of the signals being carried on the system bus 44. This can be done by tapping the system bus

44 by, for example, connecting at 170 a series of wires comprising a first tapping connection 172. Preferably, the actual number of wires in the first tapping connection 172 will be the same as the number of active wires in the system bus 44 (wires not in use can be ignored) so that, in essence, signals carried by the system bus 44 will be reproduced on the first tapping connection 172. The first tapping connection 172 is also connected to one or more transceivers 174. Preferably, transceivers 174 have a high input impedance so that degradation of the signals being carried by the system bus 44 is minimized.

Similarly, a connection is made to video device connection 52b, which may be an AGP bus for example, by connecting at 176 a second tapping connection 178 comprising the same number of active wires as the video device connection 52b (wires not in use can be ignored), so that essentially the signals carried by the video device connection 52b are reproduced on the second tapping connection 178. Again, the second tapping connection 178 is also connected to one or more transceivers 174.

Similarly, at 180, a third tapping connection 182 is connected to the hub interface bus 56, so that the signals carried by the hub interface bus 56 can be reproduced on the third tapping connection 182. Again, the third tapping connection 182 is also connected to one or more transceivers 174.

Advantageously, the transceivers 174 are unidirectional and prevent signals from the testing components 169 from interfering with the communication between components of the memory application system 38. Transceivers 174 can also strengthen the signal being transferred to other testing components 169.

Essentially, the construction of the behavioural testing system of this embodiment of the invention entails connecting a series of tapping connections to various connections of the memory application system 38, and more specifically, to connecting a tapping connection to any connection of the memory application system that provides input to or output from the system memory controller 42 connected to the system memory 46 (except

the memory bus 48, and optionally, selected unidirectional wires/ connections only carrying output from the system memory controller 42 and which are not of interest). Although Figure 4A shows only three tapping connections, the number of tapping connections will vary with the actual number of devices connected to the system memory controller 42.

By establishing tapping connections 172, 178, 182, inputs to and outputs from the system memory controller 42 may now be copied and subsequently redirected. Signals carried by the tapping connections 172, 178, 182 are directed through transceivers 174. The transceivers 174, being compatible with the signal logic levels of the signals carried by the buses 44, 52b, 56 being tapped (e.g. logic used in system bus 44 may be GTL+, logic used in video device connection 52b may be PCI, logic used in hub interface bus 56 may be LVTTL), strengthen the signals carried by tapping connections 172, 178, 182, and retransmit these signals through intermediate connections 183, 184, 185 (which carry a copy of signals carried by tapping connections 172, 178, 182 respectively) to a logic device 190.

Logic device 190 may be implemented using a field programmable gate array (FPGA), a discrete logic device, an application-specific integrated circuit (ASIC), or any programmable electronic device as is known. The logic device 190 examines the input carried by intermediate connections 183, 184, 185, and determines if the signals on any of the intermediate connections 183, 184, 185 indicate that instructions or data are being transmitted to the system memory controller 42. If so, the logic device 190 transmits a copy of the signals on intermediate connections 183, 184, 185 to a test controller 192 through test controller connections 194, 196, 198 respectively.

Preferably, test controller 192 is functionally equivalent to the system memory controller 42, and is exactly the same type of device (i.e. having the same lot number and date code) as the system memory controller 42 of the memory application system 38. Accordingly, the test controller 192 will likely behave in exactly the same manner as the system

memory controller 42 of the memory application system 38. Preferably, both system memory controller 42 and test controller 192 are "good", fully qualified devices.

Accordingly, test controller 192 will receive, through test controller connections 194, 196, 198, signals that are logically identical to those being transmitted to the system memory controller 42 in memory application system 38. The test controller 192 communicates with the memory device under test (DUT) 200 through DUT connection 202. Thus, the DUT 200 will receive instructions from the test controller 192 through DUT connection 202 in the same manner that system memory 46 of memory application system 38 receives instructions from the system memory controller 42 through the memory bus 48.

Advantageously, the combination of unidirectional transceivers 174 and logic device 190 effectively isolates the test controller 192 and the DUT 200 from the memory application system 38.

As explained above, inputs to the system memory controller 42 are effectively directed to the test controller 192. Thus, in a memory "write" cycle, data will be written to the DUT 200 in the same manner as data is written to system memory 46. In a memory "read" cycle, the data read from the DUT 200 should, if the DUT 200 has been performing in the same manner as system memory 46, be the same as the data read from system memory 46. In other words, output from the system memory controller 42 (on connecting lines except those of the memory bus 48) should be the same as output from the test controller 192 (on corresponding connecting lines except those of the DUT connection 202), if the system memory controller 42 and the test controller 192 function identically and are of the same type. Since output signals carried by connections 44, 52b and 56 of the memory application system 38 are also copied to tapping connections 172 (and 183), 178 (and 184), and 182 (and 185), the logic device 190 is able to compare output from the system memory controller 42 (on connections 183, 184, 185) with the output from the test controller 192 (on corresponding connections 194, 196, 198). The logic device 190 may

compare only the output on data lines connected to the system memory controller 42 and the corresponding output on data lines connected to the test controller 192. The logic device 190 can then direct the results of the comparison and any other output to, for example, a microcontroller 204 through microcontroller connection 206.

Again, preferably, system memory 46 which acts as a reference device is a known "good", fully qualified device that is either the same type as the DUT 200, or is functionally equivalent to the DUT 200.

Microcontroller 204 may subsequently provide the results of the comparison to the memory application system 38 itself through connection 208 to an input peripheral device 58, or to another output device, an error logging unit, a separate application system, a display, a set of LEDs, one or more error indicators (e.g. visual indicators, aural indicators, a combination of these), or an electronic component connected to one or more of these elements, for example.

Logic device 190 may also be programmed to switch from behavioural testing mode as described above, to a different testing mode. For example, other testing modes may include modes where conventional tests may be performed on a DUT 200, including pattern testing and parametric tests. The logic device 190 itself can be programmed to generate test patterns, to switch between pattern testing and behavioural testing modes, to compare the signals received by the test controller 192 in response to test pattern input or application system input, to strengthen the signals as received by the transceivers 174 where necessary, and/or to log errors found.

Microcontroller 204 can be used to control the selection of the testing mode of the logic device 190. Further, the function of the microcontroller 204, with respect to switching between testing modes, can be, for example, manually controlled, or controlled by the memory application system 38 itself through an output device 58 connected to the microcontroller 204.

Testing components 169 in the behavioural testing system

168 including the transceivers 174, the logic device 190, the controller chip 192, the DUT 200, the microcontroller 204, and most connections connecting these components may be mounted onto a testing board. As indicated earlier, the testing components 119 may be pre-combined into an add-on test device to be connected to the memory application system 38. Connections may then be made to the appropriate connections of the memory application system 38 as described above. Alternatively, the embodiment of the invention described above and illustrated schematically in Figure 4A may be implemented using two pre-manufactured circuit boards, as shown in Figure 4B. If two operational application systems 38 having similar components are available, the second application system can be converted to an add-on test device by replacing the system memory of the second application system with the DUT 200, connecting the system memory controllers from both application systems to a logic device by tapping the appropriate connections in the first application system (and providing transceivers or other electronic components as necessary), and severing the connections between the system memory controller of the second application system (which now effectively acts as the test controller) and all other components of the second application system, with the exception of the connection from the system memory controller to the DUT 200. The logic device 190 is connected to transceivers 174 and micro-controller 204 as in Figure 4A. The system memory controller 42 of the second application system essentially acts as the test controller 192 of Figure 4A. The behavioural testing system as shown in Figure 4B may be relatively easier to construct than other implementations of the more general behavioural testing system of Figure 4A since the test controller and mountings for memory devices are already installed on a board.

Referring to Figure 5, another embodiment of the invention is shown generally as 218. This embodiment expands on the embodiment of the invention described above with respect to Figure 3, in that the behavioural testing system 118 of Figure 3 has been modified to permit not only behavioural testing of the DUT 125, but also to allow the DUT 125 to be

subject to pattern testing. In Figure 5, testing components 119 now also comprises an input selector 220 which receives input from the memory application system 38 through connection 124. A test pattern generator 222 is also connected to input selector 220.

The microcontroller 139 may be used to direct the input selector 220 to switch between a pattern testing mode and a behavioural testing mode; more specifically, the input selector 220 can provide to the DUT 125 through control logic and driver device(s) 224 with either test patterns, or input originating from the memory application system 38 respectively. In this respect, the microcontroller 139 may be for example, controlled manually, or by the memory application system 38 itself through an output device 58 connected to the microcontroller 139. In both cases, the comparator 138 connected to the input selector 220 is able to compare the output of the DUT 125 (through the data receiver 136) to an expected set of data values as provided by the input selector 220.

It will be obvious to those skilled in the art that the behavioural testing systems of the various embodiments of the invention must be designed to account for the propagation delays between the various components of the behavioural testing system so as to ensure that proper comparisons are made between sets of signals being compared. This will typically be necessary if all components of the behavioural testing system are synchronized to one clock signal.

Referring to Figure 6, the steps of a method of testing memory devices in accordance with a preferred embodiment of the present invention are shown, the method commencing at step 250.

The method of testing a memory device proceeds to step 252 where the mode of test is selected. In this embodiment of the present invention illustrated in Figure 6, only a pattern testing mode or a behavioural testing mode may be selected, and only one mode may be selected at a given time. It will be obvious to those skilled in the art however, that in other embodiments of the present invention, other testing modes including modes where other conventional tests are performed, may be incorporated

in the method.

At step 254, if the pattern testing mode has been selected, (by, for example, a microcontroller 204 (Figure 4A), 139 (Figure 5)), the flow of method steps proceeds to step 255 where pattern tests are applied to a memory device under test (DUT).

Pattern testing may continue for a specified duration, until all generated test patterns have been applied, or until all pre-selected test patterns have been applied. At step 256, if the DUT is to be subjected to further testing, the flow of method steps proceeds back to step 252 at which another testing mode may be selected, otherwise the flow of method steps proceeds to step 257 marking the end of the method of testing a memory device.

If at step 254, pattern testing mode was not selected, step 258 is performed at which the controller determines if behavioural testing mode has been selected. If so, the flow of method steps proceeds to step 260 at which behavioural testing is performed; that is, inputs originating from an application system are applied to the DUT. When the behavioural tests are completed (e.g. after a specified duration, upon manual termination, or upon the occurrence of a pre-specified event), the flow of method steps proceeds to step 256 described above.

Figures 7A and 7B represent two alternative embodiments of a method of behavioural testing in which behavioural tests are performed on a DUT. Behavioural tests may be performed at step 260 of Figure 6.

Referring first to Figure 7A, the method of behavioural testing, which may be performed using a behavioural testing system with an architecture similar to that of the behavioural testing system 168 of Figure 4A, commences at step 300a.

At step 310a, a copy of all signals being transmitted to a system memory controller connected to system memory (preferably, signals being transmitted to the system memory controller on the memory bus are exempted) is redirected through one or more testing components to a test controller connected to the DUT.

At step 320a, signals that are transmitted by the system memory controller (preferably, the signals that are outputted from the system memory controller not including the output to system memory) are compared to signals that are transmitted by the test controller (preferably, the signals that are outputted from the test controller not including the output to the DUT) using, for example, a logic device.

At step 330a, the results of the comparison are outputted, for example, to a microcontroller, or directly to one or more other output devices or electronic components.

At step 340a, if there has been an indication that behavioural testing should be ended, the flow of method steps proceeds to step 350a which marks the end of the method, otherwise, the flow of method steps proceeds to step 310a at which the steps of the method are repeated.

Referring to Figure 7B, another embodiment of the method of behavioural testing in accordance with the present invention commences at step 300b. This embodiment of the behavioural testing method in which behavioural tests are performed, can be used in a behavioural testing system with an architecture similar to that of the behavioural testing system 218 of Figure 5 (or behavioural testing system 118 of Figure 3).

At step 310b, a copy of all signals being transmitted to system memory is redirected through one or more testing components to the memory device under test (DUT).

At step 320b, a copy of data read from system memory is compared with data read from the DUT.

Data may be written into system memory and the DUT multiple times at step 310b, before data is read from system memory or the DUT at step 320b.

At step 330b, the results of the comparison are outputted, as in step 330a of Figure 7A.

At step 340b, if there has been an indication that behavioural testing should be ended, the flow of method steps proceeds to step 350b which marks the end of the method, otherwise, the flow of method steps

proceeds to step 310b at which the steps of the method are repeated.

Advantageously, the DUT is accordingly subject to the same operations, and the same order of operations, as the system memory is subject to while operating in its actual operating environment within an application system.

While the systems of Figures 3 or 5 may be easier to construct than the system of Figure 4A, it is noted that the DUT 125 of Figures 3 and 5 receives signals that are independent of the type of controller connected to system memory. As a memory device may operate differently depending on the type of controller which it is attached to (due to impedance mismatches between the output of the controller chip and the input to the memory device), some characteristics of the signals being directed to the DUT may not be exactly the same as those being transmitted to system memory, since the DUTs of Figures 3 and 5 are not connected to a controller. For example, impedance mismatches between a controller and a connected memory device may cause signals being transmitted to the memory device to undershoot or overshoot the desired voltage level. These deviations from the desired voltage level may, on some occasions, cause an error in the output of the memory device. Therefore, the system of Figure 4A, in which a controller is connected to the DUT, may provide for a greater degree of accuracy in behavioural testing, if the test controller 192 behaves substantially the same as the system memory controller 42, which is likely to be the case if the test controller 192 and the system memory controller 42 are functionally equivalent and are of the same type (e.g. having the same lot numbers and date codes).

Some devices in the systems described herein including, for example, the test pattern generator, the data receiver, and the comparator, may be implemented using a microprocessor programmed to perform the desired function, or alternatively in a state machine implemented on a chip, in a logic circuit connected to a memory device, using any combination of the above, or using any suitable implementation as is known.

It will be obvious to those skilled in the art that the memory

device under test may be comprised of a single memory chip or multiple memory chips or memory modules.

In variant embodiments of the invention, the results of comparisons between expected data and data obtained from a device under test (as performed in step 320a of Figure 7A and in step 320b of Figure 7B) may also be logged in an error logging unit.

In variant embodiments of the invention, instead of tapping the memory bus of Figure 3 or Figure 5 by making a direct wire connection to the wires of the memory bus, one or more of the system memory modules may be mounted on a board. Also mounted on this board are drivers connected to the control, address, and data lines of the memory bus which drive the signals on those lines through a cable (e.g. an LVDS cable) to a series of transceivers and/or drivers, directing the signals to the testing components. One such alternative arrangement and apparatus for tapping a memory bus is illustrated in Figure 8.

In variant embodiments of the invention, the reliability, accuracy and scope of tests applied to a device under test may be further improved by providing a means to vary various operating parameters with respect to selected testing components and the device under test. In this embodiment, parametric tests are performed whereby testing is conducted under a range of different operating parameters, including tests performed at the extremes of those ranges. A behavioural testing system may be adapted to allow parametric testing to be performed in a separate testing mode.

For example, referring to Figure 9, a parametric control device 400 has been added to the behavioural testing system of Figure 5. The parametric control device 400 can be connected to the DUT 125 to vary a number of operating parameters, including for example: V_{DD}, V_{DDQ}, V_{TT}, V_{REF}. The parametric control device 400 can also be connected to the driver 224 connected to the DUT 125 to vary a number of operating parameters, including for example: setup/hold time, driver strength, skew rate, signal

rise/fall time, V_{OL}, V_{OH}. The parametric control device 400 can also be connected to the data receiver 136 to vary a number of operating parameters, including for example: read strobe timing, V_{IH}, V_{IL}. By varying the operating parameters within a range that is consistent with what the testing components may face in a real application system, a more comprehensive test of the devices under test can be achieved.

In variant embodiments of the invention, the reliability, accuracy and scope of tests applied to a device under test may be further improved by providing a means to vary various electrical operating conditions under which the behavioural testing system operates (e.g. temperature, humidity). In this embodiment, behavioural tests are performed whereby testing is conducted under a range of different operating conditions, including tests performed at the extremes of those ranges. This method of testing may be referred to as environmental testing.

In variant embodiments of the invention, with respect to some of the components of the behavioural testing systems, it will be apparent to those skilled in the art that the functions of these components need not be performed by the particular component specified in the description. For example, it will be obvious to those skilled in the art that the functions of the logic device 190 of Figure 4A may be performed by several electronic components, and need not be limited to being performed by a single electronic device. As a further example, it will also be obvious to those skilled in the art that the functions of several devices as described in the specification may be combined so as to be performed by a fewer number (at least one) electronic component.

In variant embodiments of the invention, the memory application system may not be limited to a personal computer, but may also be for example, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses a memory device, or in fact, any electronic device, system, or box that uses a memory device.

Referring to Figure 10 which illustrates a system in a variant embodiment of the invention, more than one set of testing components can be supplied with the tapped signals from an application system, and with the aid of one or more transceivers and/or logic devices, many devices can be simultaneously tested in parallel.

In variant embodiments of the invention, the device under test is an integrated circuit device that has been previously untested having come directly off of a manufacturing line, or that has been previously classified as failed or rejected by its manufacturer. While a device may initially be rejected by its manufacturer for failing to meet stringent general specifications, the device may still be suitable for a particular application that requires devices that can meet less stringent specifications. Thus, applying behavioural tests to a device under test, and applying these tests while varying the various operating parameters within a range more specifically suited to the device's intended application, a previously failed or rejected device may pass the behavioural tests and be found to be suitable for the specific application. Thus, behavioural tests are particularly useful for reclassifying previously failed or rejected devices, and the present invention thus provides for a method and system that may also be used to test such previously failed or rejected devices to ensure that they are likely to function normally under a specific application.

In variant embodiments of the invention, the systems and methods described in this specification are not limited to the testing of memory devices (e.g. SDRAM, SRAM, DRAM, EDORAM, etc.) in memory application systems, but the invention may also be adapted to test processor chips, application-specific integrated circuit (ASIC) chips, data com devices, components, boxes, or in fact any type of integrated circuit device in any application system. The invention may be generally applied by locating a system electronic component operating within an application system that is similar to the device under test, tapping connections carrying signals being transmitted to that system electronic component, directing a copy of those signals to the device under test, and comparing the signals

transmitted from the system electronic component with the signals transmitted from the device under test to determine if the device under test is working properly.

Alternatively, the invention may be applied by locating a system controller or one or more other electronic components connected to the system electronic component in an application system, tapping connections carrying signals transmitted to and from that system controller or one or more electronic components, directing a copy of those signals to a test controller or one or more test components connected to the device under test (where the test controller or one or more test components is/are of the same type and has/have the same function as the system controller or one or more electronic components), and comparing the signals transmitted by the system controller or one or more electronic components to the signals transmitted by the test controller or one or more test components to determine if the device under test performs as expected.

In variant embodiments of the invention, a behavioural testing system of the present invention may be initially constructed by modifying a conventional testing system in which only conventional tests are performed on a device under test. For example, the test pattern generator of a prior art conventional testing system as shown in Figure 1 may be replaced by one or more components or devices capable of providing input from an application system to construct a behavioural testing system of the present invention.

In variant embodiments of the invention, the behavioural testing systems and methods of the present invention may be modified to allow a device under test to be tested using signals originating from an actual application system, without requiring the application system to be operating while the device under test is being tested. For example, signals on system connections in an application system that would be applied to a device under test (or to a controller or other component connected to the device under test) according to the preferred embodiments of the invention by tapping the appropriate system connections and directing a copy of the

signals on those connections to the device under test (or to a controller or other component connected to the device under test), may instead be stored in a memory or storage device. In essence, test signals generated by the application system are captured or recorded in the memory or storage device for subsequent use. The stored test signals may then be applied to the device under test using, for example, a driver or a logic device. As a result, in these variant embodiments of the invention, the application system need not necessarily be a part of the behavioural testing system during the testing of the device under test. However, the device under test is still subjected to behavioural tests as signals originating from an actual application system are still used to test the device under test, thus exposing the device under test to conditions representative of what the device might be required to operate under when it is ultimately used in its intended application environment. Examples of variant embodiments of behavioural testing systems designed in accordance with the present invention are illustrated in Figures 11A, 11B, 11C and 11D, which are modifications of the systems of Figures 3, 4A, 5 and 9 respectively. In these variant embodiments of the invention, signals generated by an application system are received by the test components from a memory device 410 rather than from a connected application system. Nonetheless, the memory device 410 still provides testing components 119 (Figures 11A, 11C, 11D), 169 (Figure 11B) with signals generated from an actual application system to be applied to a device under test 125 (Figures 11A, 11C, 11D), or a test controller 192 (Figure 11B), and to be compared with the output of the device under test 125 or test controller 192. The microcontroller 139 (Figures 11A, 11C, 11D), 204 (Figure 11B) may receive input from or provide output to other devices through an I/O connection 411.

In variant embodiments of the invention, test signals representative of actual signals in an application system may be modeled or simulated by a simulation device, and subsequently stored in a memory or storage device. The stored test signals may then be applied to the device under test using, for example, a driver or a logic device.

As will be apparent to those skilled in the art, other various modifications and adaptations of the systems and methods described herein are possible without departing from the present invention, the scope of which is defined in the claims.

WE CLAIM:

1. A behavioural testing system for testing an electronic component, the electronic component being the device under test, the system comprising:

(a) an application system in which a test signal is generated, the test signal to be applied to both a reference device in the application system and the device under test, the reference device being of the same type or functionally equivalent to the device under test;

(b) tapping connections connected to system connections in the application system, the system connections being connected to the reference device;

(c) testing components connected to said tapping connections for applying the test signal to the device under test;

(d) a device for comparing the signals received in response to the test signal from the reference device with the signals received in response to the test signal from the device under test; and

(e) means for indicating the results of the comparison.

2. The system as claimed in claim 1, wherein said testing components comprises at least one transceiver connected to said tapping connections and to the other testing components.

3. The system as claimed in claim 2, wherein the at least one transceiver is used to minimize the effect on the integrity of signals being carried on the system connections, and to isolate the other testing components and the device under test from the application system.

4. The system as claimed in claim 1, wherein the system also comprises a device for applying conventional tests to the device under test.

5. The system as claimed in claim 4, wherein the device for applying conventional tests to the device under test is a device that generates test patterns.

6. The system as claimed in claim 4, wherein the device for applying conventional tests to the device under test is a parametric control device.

7. A behavioural testing system for testing an electronic component, the electronic component being the device under test, the system comprising:

(a) an application system in which an input signal is generated, wherein the input signal is applied to both a system controller and a test controller, wherein the system controller is connected to a reference device in the application system, wherein the system controller generates a first test signal which is applied to the reference device in response to the input signal, wherein the test controller is connected to the device under test, wherein the test controller generates a second test signal which is applied to the device under test in response to the input signal, and wherein the reference device is of the same type or is functionally equivalent to the device under test;

(b) tapping connections connected to system connections in the application system, the system connections being connected to the system controller;

(c) testing components connected to said tapping

connections for applying the test signal to the test controller;

(d) a device for comparing the signals received in response to the input signal from the system controller with the signals received in response to the input signal from the test controller; and

(e) means for indicating the results of the comparison.

8. The system as claimed in claim 7, wherein said testing components comprises at least one transceiver connected to said tapping connections and to the other testing components.

9. The system as claimed in claim 8, wherein the at least one transceiver is used to minimize the effect on the integrity of signals being carried on the system connections, and to isolate the other testing components and the device under test from the application system.

10. The system as claimed in claim 7, wherein the system also comprises a device for applying conventional tests to the device under test.

11. The system as claimed in claim 10, wherein the device for applying conventional tests to the device under test is a device that generates test patterns.

12. The system as claimed in claim 10, wherein the device for applying conventional tests to the device under test is a parametric control device.

13. The system as claimed in claim 7, wherein the test controller is a system controller of a second application system.

14. A behavioural testing system for testing an electronic

component, the system comprising:

(a) an application system in which at least one test signal is generated;

(b) a reference device in the application system;

(c) an electronic component, the electronic component being the device under test;

(d) testing components connected to the application system and the electronic component, the testing components adapted to direct a plurality of signals from the application system to the electronic component, and wherein the application system will not fail if the electronic components fails; and

(e) means for comparing the output from the reference device and the electronic component.

15. The system of claim 14, wherein the electronic component is one of the following: a memory chip, an application-specific integrated circuit chip, a processor chip, a data com device, an electronic device.

16. The system of claim 14, wherein the testing components comprises at least one transceiver.

17. The system of claim 15, wherein the electronic component is a memory chip for use in at least one of the following: a personal computer, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses at least one memory chip, an electronic device that uses at least one memory chip, an electronic system that uses at least one memory chip, an electronic box that uses at least one memory chip.

18. The system as claimed in claim 14, wherein the system also

comprises a device for applying conventional tests to the device under test.

19. The system as claimed in claim 18, wherein the device for applying conventional tests to the device under test is a device that generates test patterns.

20. The system as claimed in claim 18, wherein the device for applying conventional tests to the device under test is a parametric control device.

21. A behavioural testing method for testing an integrated circuit device wherein:

(a) a first integrated circuit device is provided with an input, said input comprising a copy of a plurality of signals communicated to a second integrated circuit device of an application system; and

(b) signals provided by the first integrated circuit device in response to said input are compared to the signals provided by the second integrated circuit device in response to the signals communicated to the second integrated circuit device.

22. The method as claimed in claim 21, wherein each of the first and second integrated circuit devices is one of the following: a memory chip, an application-specific integrated circuit chip, a processor chip, a data com device, an electronic component.

23. The method as claimed in claim 22, wherein said application system is one of the following: a personal computer, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses at least one

memory chip, an electronic device that uses at least one memory chip, an electronic system comprising at least one memory chip, an electronic box comprising at least one memory chip.

24. The method as claimed in claim 22, wherein a plurality of first integrated circuit devices are tested in parallel.

25. The method as claimed in claim 21, wherein the method also comprises the step of applying conventional tests to the device under test.

26. The method as claimed in claim 25, wherein the step of applying conventional tests to the device under test includes applying test patterns to a device under test.

27. The method as claimed in claim 25, wherein the step of applying conventional tests to the device under tests includes modifying the operating parameters of at least one testing component.

28. The method as claimed in claim 21, wherein said first integrated circuit device is a device that has been previously classified as failed or rejected by its manufacturer.

29. The method as claimed in claim 21, also comprising the step of outputting the results of the comparison in step (b).

30. The method as claimed in claim 29, wherein the results of the comparison are represented on at least one of: a display, one or more light-emitting diodes, one or more error indicators, an output device.

31. The method as claimed in claim 29, wherein the results of the comparison are stored in one of: a memory device, a storage device.

32. The method as claimed in claim 29, wherein the results of the comparison are directed to one of: a logic device, a processor, an application system, a microcontroller, a network.

33. A method for testing an integrated circuit device, said method comprising:

(a) transmitting a first plurality of signals to a first integrated circuit device, said first integrated circuit device being the device under test, said first plurality of signals being logically identical to a second plurality of signals transmitted to a second integrated circuit device operating in an application system;
(b) determining a first response by the first integrated circuit device to at least one of said first plurality of signals;
(c) determining a second response by the second integrated circuit device to at least one of said second plurality of signals; and
(d) comparing said first and second responses.

34. The method as claimed in claim 33, wherein the first plurality of signals is obtained by tapping the connections between said second integrated circuit device and any other component in said application system, and copying the signals carried by those connections.

35. The method as claimed in claim 34, wherein each of the first and second integrated circuit devices is one of the following: a memory chip, an application-specific integrated circuit chip, a processor chip, a data com device, an electronic component.

36. The method as claimed in claim 35, wherein said application system comprises at least one electronic circuit, and wherein one of said at

least one electronic circuit either contains or is connected to said second integrated circuit device.

37. The method as claimed in claim 36, wherein said application system is one of the following: a personal computer, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses at least one memory chip, an electronic device that uses at least one memory chip, an electronic system comprising at least one memory chip, an electronic box comprising at least one memory chip.

38. The method as claimed in claim 33, also comprising the step of outputting the results of the comparison in step (d).

39. The method as claimed in claim 38, wherein the results of the comparison are represented on at least one of: a display, one or more light-emitting diodes, one or more error indicators, an output device.

40. The method as claimed in claim 38, wherein the results of the comparison are stored in one of: a memory device, a storage device.

41. The method as claimed in claim 38, wherein the results of the comparison are directed to one of: a logic device, a processor, an application system, a microcontroller, a network.

42. The method as claimed in claim 35, wherein a plurality of first integrated circuit devices are tested in parallel.

43. The method as claimed in claim 33, wherein the method also comprises the step of applying conventional tests to the device under test.

44. The method as claimed in claim 43, wherein the step of

applying conventional tests to the device under test includes applying test patterns to a device under test.

45. The method as claimed in claim 43, wherein the step of applying conventional tests to the device under tests includes modifying the operating parameters of at least one testing component.

46. The method as claimed in claim 33, wherein said first integrated circuit device is a device that has been previously classified as failed or rejected by its manufacturer.

47. A method for testing an integrated circuit device, said method comprising:

(a) transmitting a first plurality of signals to a first controller, said first controller being connected to a first integrated circuit device, said first integrated circuit device being the device under test, said first plurality of signals being logically identical to a second plurality of signals transmitted to a second controller, said second controller being connected to a second integrated circuit device, said second controller and said second integrated circuit device operating in an application system;
(b) determining a first response by the first controller to at least one of said first plurality of signals;
(c) determining a second response by the second controller to at least one of said second plurality of signals; and
(d) comparing said first and second responses.

48. The method as claimed in claim 47, wherein said first and second controllers are functionally equivalent.

49. The method as claimed in claim 47, wherein the first plurality of signals is obtained by tapping at least one connection between said second controller and a component other than the second integrated circuit device in said application system.

50. The method as claimed in claim 49, wherein each of the first and second integrated circuit devices is one of the following: a memory chip, an application-specific integrated circuit chip, a processor chip, a data com device, an electronic component.

51. The method as claimed in claim 50, wherein said application system comprises at least one electronic circuit, and wherein one of said at least one electronic circuit either contains or is connected to said second integrated circuit device.

52. The method as claimed in claim 50, wherein said application system is one of the following: a personal computer, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses at least one memory chip, an electronic device that uses at least one memory chip, an electronic system comprising at least one memory chip, an electronic box comprising at least one memory chip.

53. The method as claimed in claim 47, also comprising the step of outputting the results of the comparison in step (d).

54. The method as claimed in claim 53, wherein the results of the comparison are represented on at least one of: a display, one or more light-emitting diodes, one or more error indicators, an output device.

55. The method as claimed in claim 53, wherein the results of the comparison are stored in one of: a memory device, a storage device.

56. The method as claimed in claim 53, wherein the results of the comparison are directed to one of: a logic device, a processor, an application system, a microcontroller, a network.

57. The method as claimed in claim 50, wherein a plurality of first integrated circuit devices are tested in parallel.

58. The method as claimed in claim 47, wherein the method also comprises the step of applying conventional tests to the device under test.

59. The method as claimed in claim 58, wherein the step of applying conventional tests to the device under test includes applying test patterns to a device under test.

60. The method as claimed in claim 58, wherein the step of applying conventional tests to the device under tests includes modifying the operating parameters of at least one testing component.

61. The method as claimed in claim 47, wherein said first integrated circuit device is a device that has been previously classified as failed or rejected by its manufacturer.

62. A system for testing an integrated circuit device, the system comprising:

(a) a first integrated circuit device, said first integrated circuit device being the device under test;
(b) a second integrated circuit device operating in an application system;
(c) a plurality of system connections connecting the second integrated circuit device to other components in said

application system;

(d) a plurality of test components, said plurality of test components connected to said first integrated device and to said plurality of system connections, said plurality of test components adapted to direct signals carried by the plurality of system connections to the first integrated circuit device; and

(e) a comparator for comparing the responses by the first and second integrated circuit devices to said signals.

63. The system as claimed in claim 62, wherein each of the first and second integrated circuit devices is one of the following: a memory chip, an application-specific integrated circuit chip, a processor chip, a data com device, an electronic component.

64. The system as claimed in claim 63, wherein said application system comprises at least one electronic circuit, and wherein one of said at least one electronic circuit either contains or is connected to said second integrated circuit device.

65. The system as claimed in claim 63, wherein said application system is one of the following: a personal computer, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses at least one memory chip, an electronic device that uses at least one memory chip, an electronic system comprising at least one memory chip, an electronic box comprising at least one memory chip.

66. The system as claimed in claim 62, wherein the system also comprises a device for applying conventional tests to the device under test.

67. The system as claimed in claim 66, wherein the device for

applying conventional tests to the device under test is a device that generates test patterns.

68. The system as claimed in claim 66, wherein the device for applying conventional tests to the device under test is a parametric control device.

69. The system as claimed in claim 66, wherein said system also comprises an input selector device adapted to switch between providing input to said first integrated circuit device from said device for applying conventional tests to the device under test, and providing signals being carried by the plurality of system connections to said first integrated circuit device.

70. The system as claimed in claim 62, wherein said system also comprises an error logging unit connected to said comparator, said error logging unit adapted to direct the results of the comparison to at least one of: a microcontroller, a network, a display, one or more light-emitting diodes, one or more error indicators, a processor, an application system, a logic device, a storage device, an output device, a memory device.

71. A system for testing an integrated circuit device, said system comprising:

(a) a first integrated circuit device, the first integrated circuit device being the device under test;
(b) a first controller connected to said first integrated circuit device;
(c) a second integrated circuit device operating in an application system;
(d) a second controller connected to said second integrated circuit device, said second controller operating in said

application system;

(e) a plurality of system connections connecting said second controller to other components in said application system other than the second integrated circuit device;

(f) a plurality of test components comprising at least one electronic component and connections, said plurality of test components connected to said first controller and to said plurality of system connections, said plurality of test components adapted to direct signals carried by the plurality of system connections to said first controller; and

(g) a comparator adapted to compare the responses to said signals by the first and second controllers.

72. The system as claimed in claim 71, wherein said first and second controllers are functionally equivalent.

73. The system as claimed in claim 71, wherein each of the first and second integrated circuit devices is one of the following: a memory chip, an application-specific integrated circuit chip, a processor chip, a data com device, an electronic component.

74. The system as claimed in claim 73, wherein said application system comprises at least one electronic circuit, and wherein one of said at least one electronic circuit either contains or is connected to said second integrated circuit device.

75. The system as claimed in claim 74, wherein said application system is one of the following: a personal computer, a video game, a voice recorder, a network server, a digital television, an MP3 player, a camera, a cellular phone, a microprocessor-based device which uses at least one memory chip, an electronic device that uses at least one memory chip, an electronic system comprising at least one memory chip, an electronic box

comprising at least one memory chip.

76. The system as claimed in claim 71, wherein the system also comprises a device for applying conventional tests to the device under test.

77. The system as claimed in claim 76, wherein the device for applying conventional tests to the device under test is a device that generates test patterns.

78. The system as claimed in claim 76, wherein the device for applying conventional tests to the device under test is a parametric control device.

79. The system as claimed in claim 76, wherein said system also comprises an input selector device adapted to switch between providing input from said device for applying conventional tests to the device under test, and providing signals being carried by the plurality of system connections to one of the first integrated circuit device and the first controller.

80. The system as claimed in claim 71, wherein said system also comprises an error logging unit connected to said comparator, said error logging unit adapted to direct the results of the comparison to at least one of: a microcontroller, a network, a display, one or more light-emitting diodes, one or more error indicators, a processor, an application system, a logic device, a storage device, an output device, a memory device.

81. A system for testing an integrated circuit device, the system comprising:

(a) a test device;
(b) a storage device for test signals;
(c) a plurality of test components, said plurality of test components connected to said test device and said

storage device, said plurality of test components adapted to direct a first plurality of signals stored in said storage device to said test device; and

(d) a comparator for comparing the output of said test device with a second plurality of signals stored in said storage device.

82. The system as claimed in claim 81, wherein said test signals are one of:

(a) copies of system signals originating from an application system, said system signals comprising inputs to a component of the application system and outputs from said component of the application system, said component of the application system being of the same type as said test device or functionally equivalent to said test device; or

(b) simulation signals generated by a simulation device, wherein said simulation signals simulate system signals originating from an application system, said system signals comprising inputs to a component of the application system and outputs from said component of the application system, said component of the application system being of the same type as said test device or functionally equivalent to said test device.

83. The system as claimed in claim 82, wherein the test device is an integrated circuit device, said integrated circuit device being the device under test.

84. The system as claimed in claim 82, wherein the test device is a controller connected to an integrated circuit device, said integrated circuit device being the device under test.

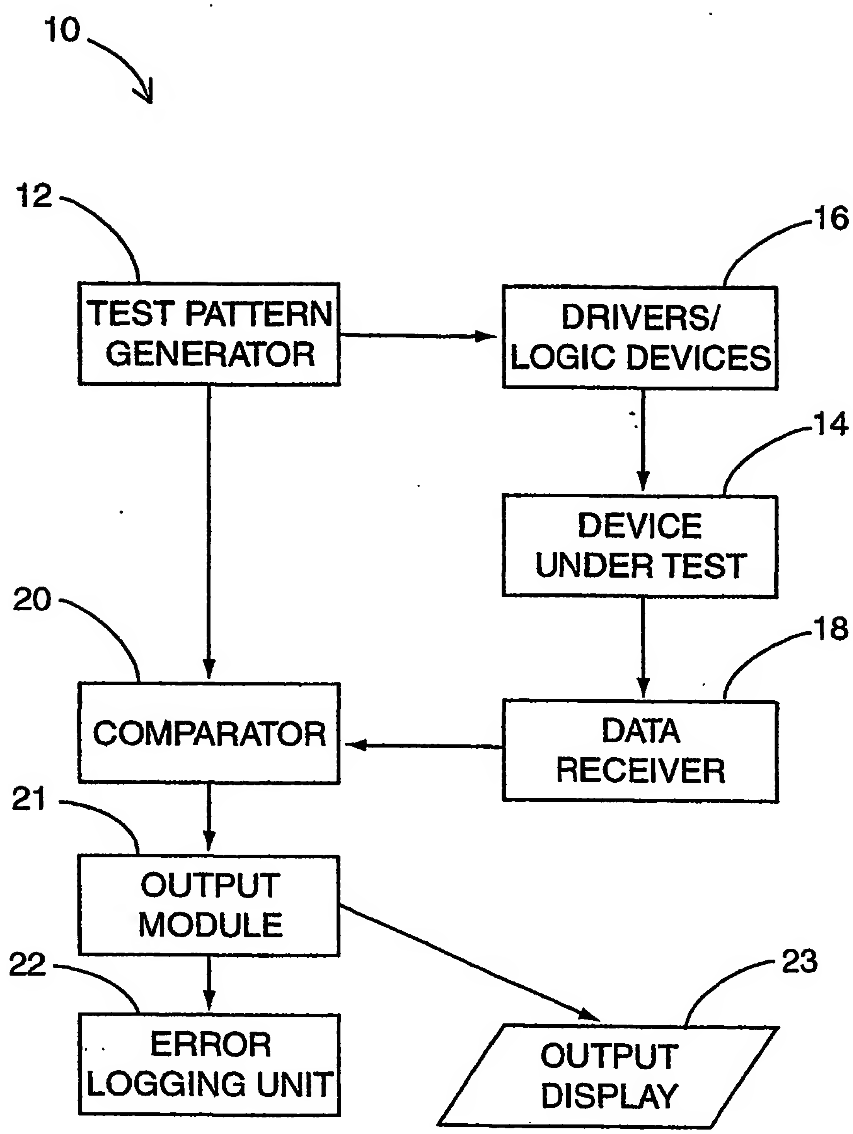


FIG. 1
PRIOR ART

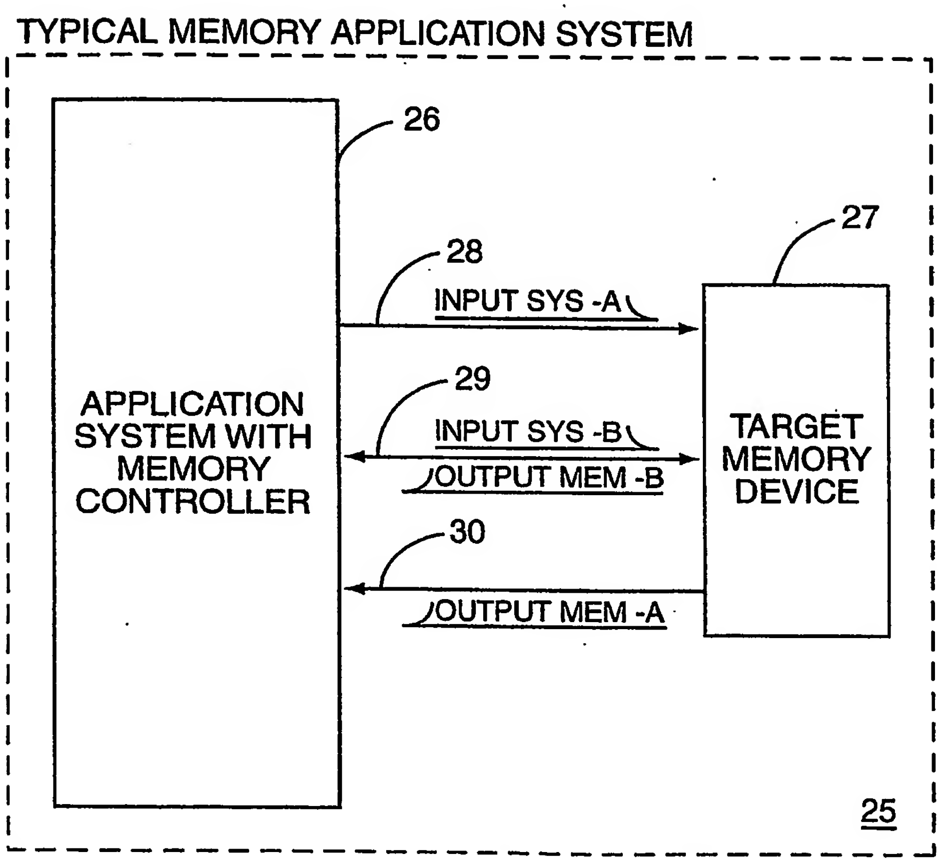


FIG. 2A
PRIOR ART

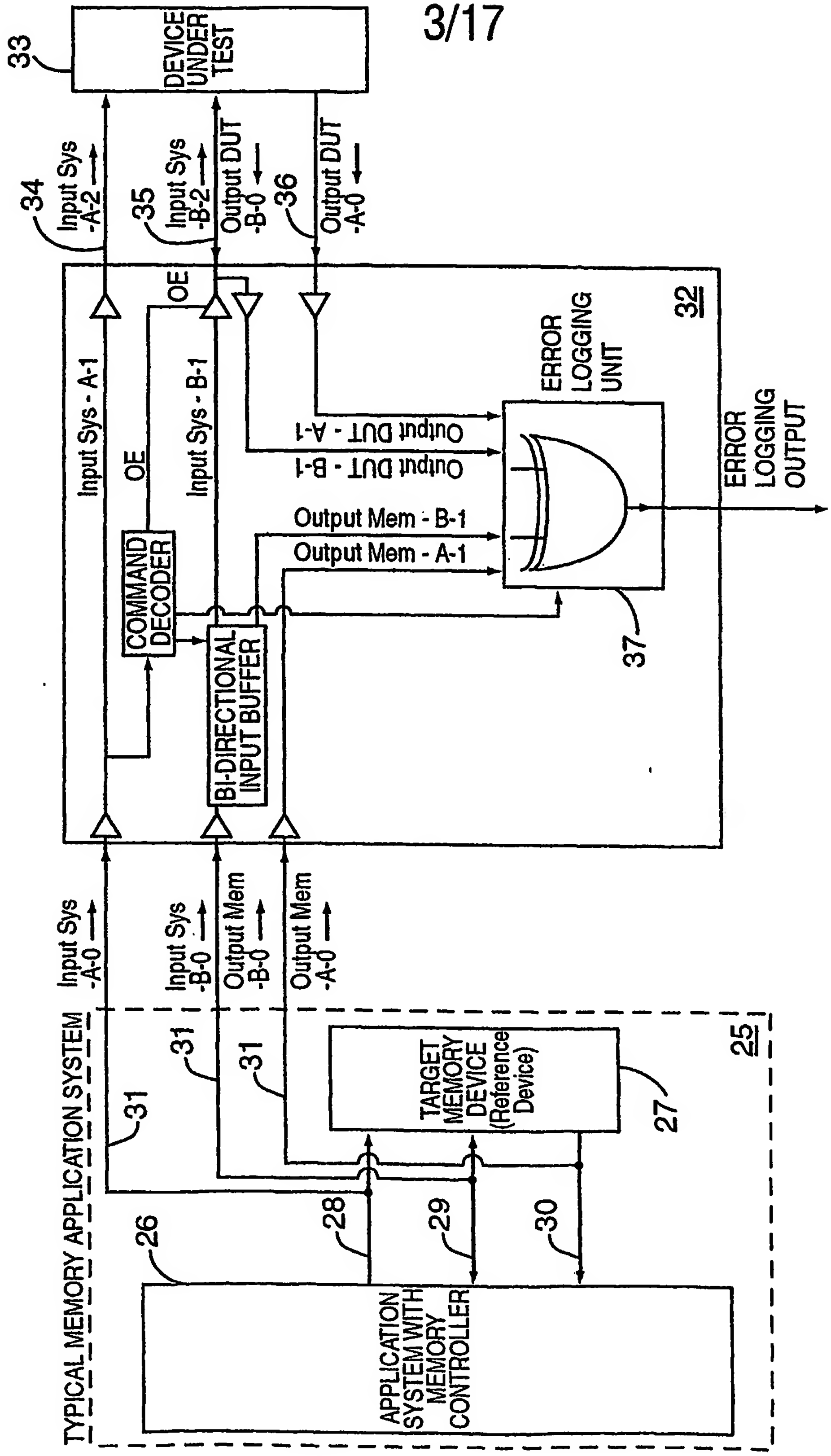

DEVICE UNDER TEST
33
34
Input Sys -A-2
35
Input Sys -B-2
Output DUT -B-0
36
Output DUT -A-0
Input Sys - A-1
OE
Input Sys - B-1
OE
COMMAND DECODER
BI-DIRECTIONAL INPUT BUFFER
Output DUT - A-1
Output DUT - B-1
Output Mem - B-1
Output Mem - A-1
ERROR LOGGING UNIT
ERROR LOGGING OUTPUT
32
37
Input Sys -A-0
Input Sys -B-0
Output Mem -B-0
Output Mem -A-0
TYPICAL MEMORY APPLICATION SYSTEM
31
31
31
TARGET MEMORY DEVICE (Reference Device)
27
25
26
28
29
30
APPLICATION SYSTEM WITH MEMORY CONTROLLER

FIG. 2B

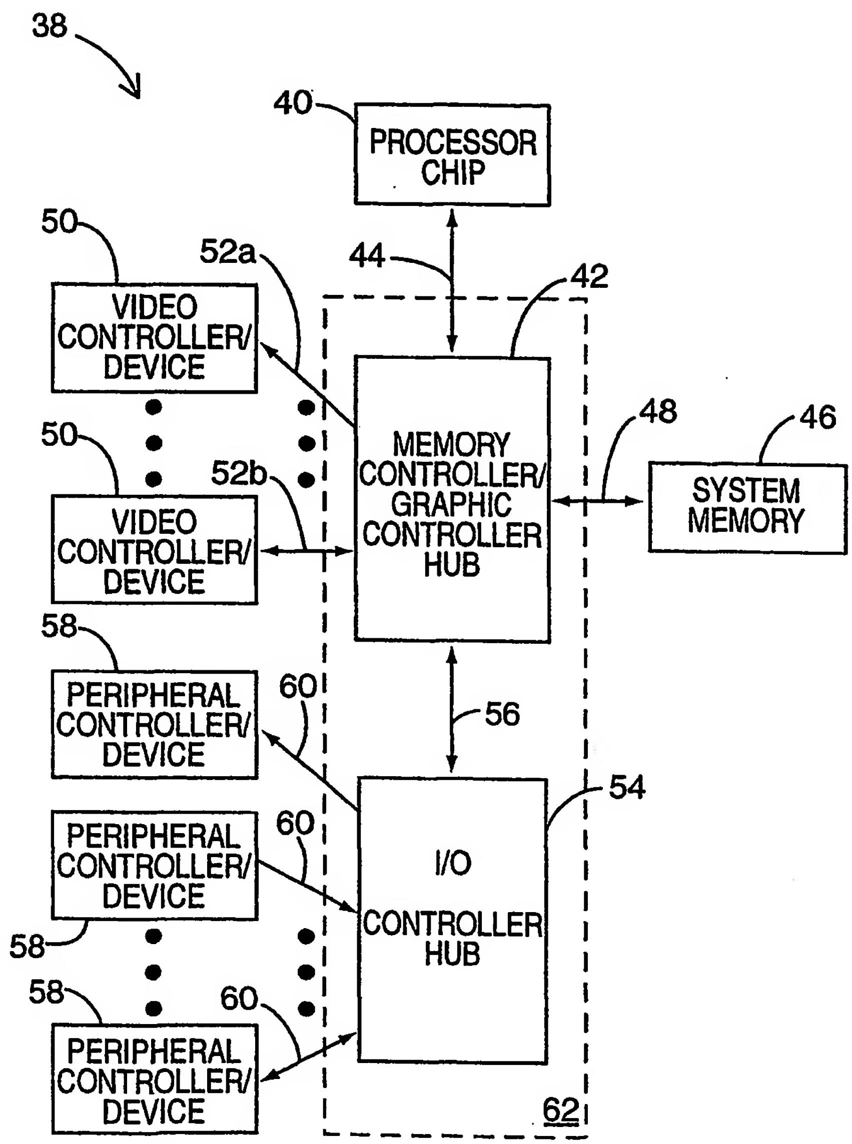
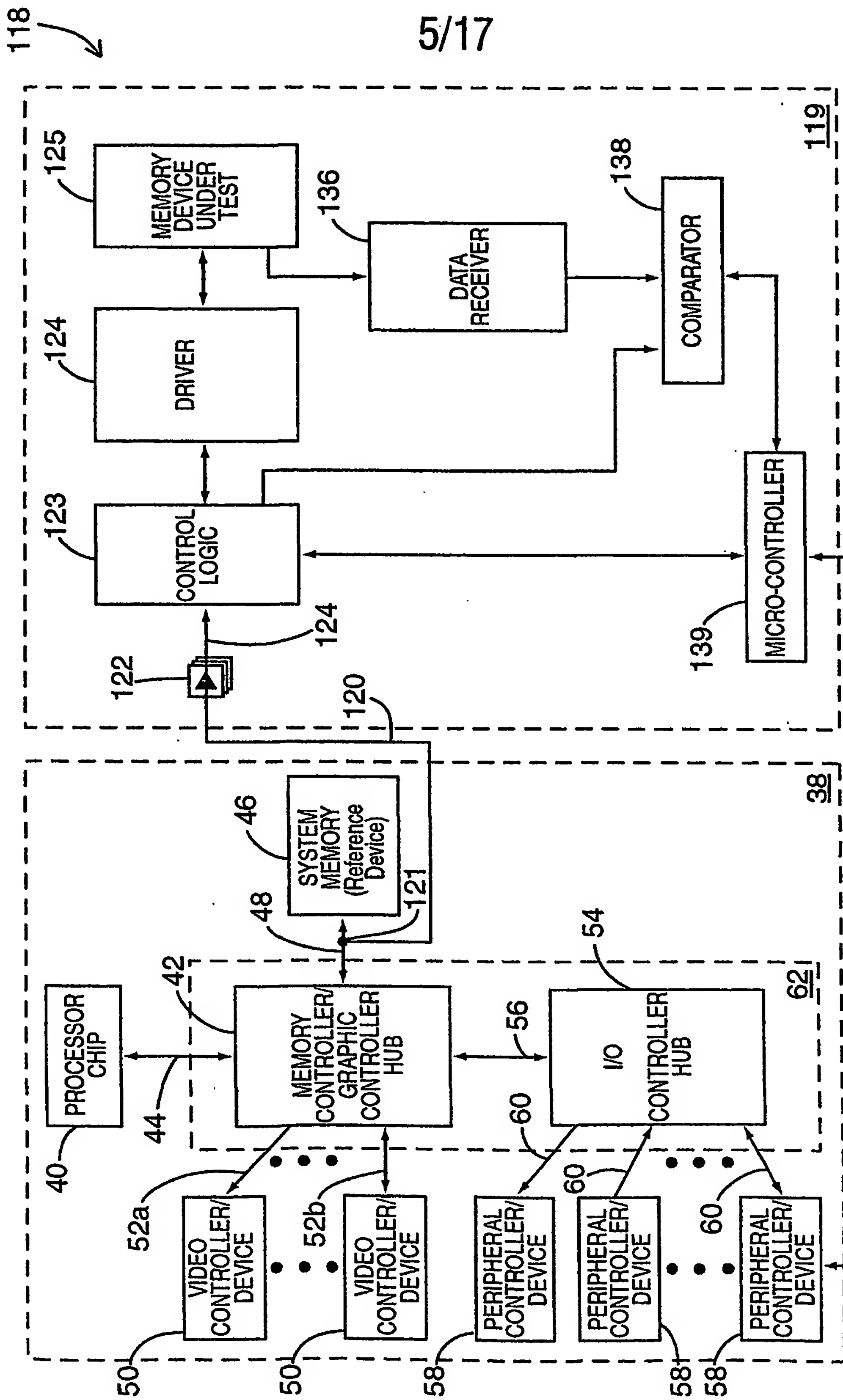


FIG. 2C
PRIOR ART



118
119
MEMORY DEVICE UNDER TEST
125
DRIVER
124
CONTROL LOGIC
123
DATA RECEIVER
136
COMPARATOR
138
MICRO-CONTROLLER
139
122
124
120
38
SYSTEM MEMORY (Reference Device)
46
121
48
PROCESSOR CHIP
40
44
MEMORY CONTROLLER/ GRAPHIC CONTROLLER HUB
42
56
I/O CONTROLLER HUB
54
62
140
VIDEO CONTROLLER/ DEVICE
52a
52b
50
50
PERIPHERAL CONTROLLER/ DEVICE
60
60
60
58
58
58

FIG. 3

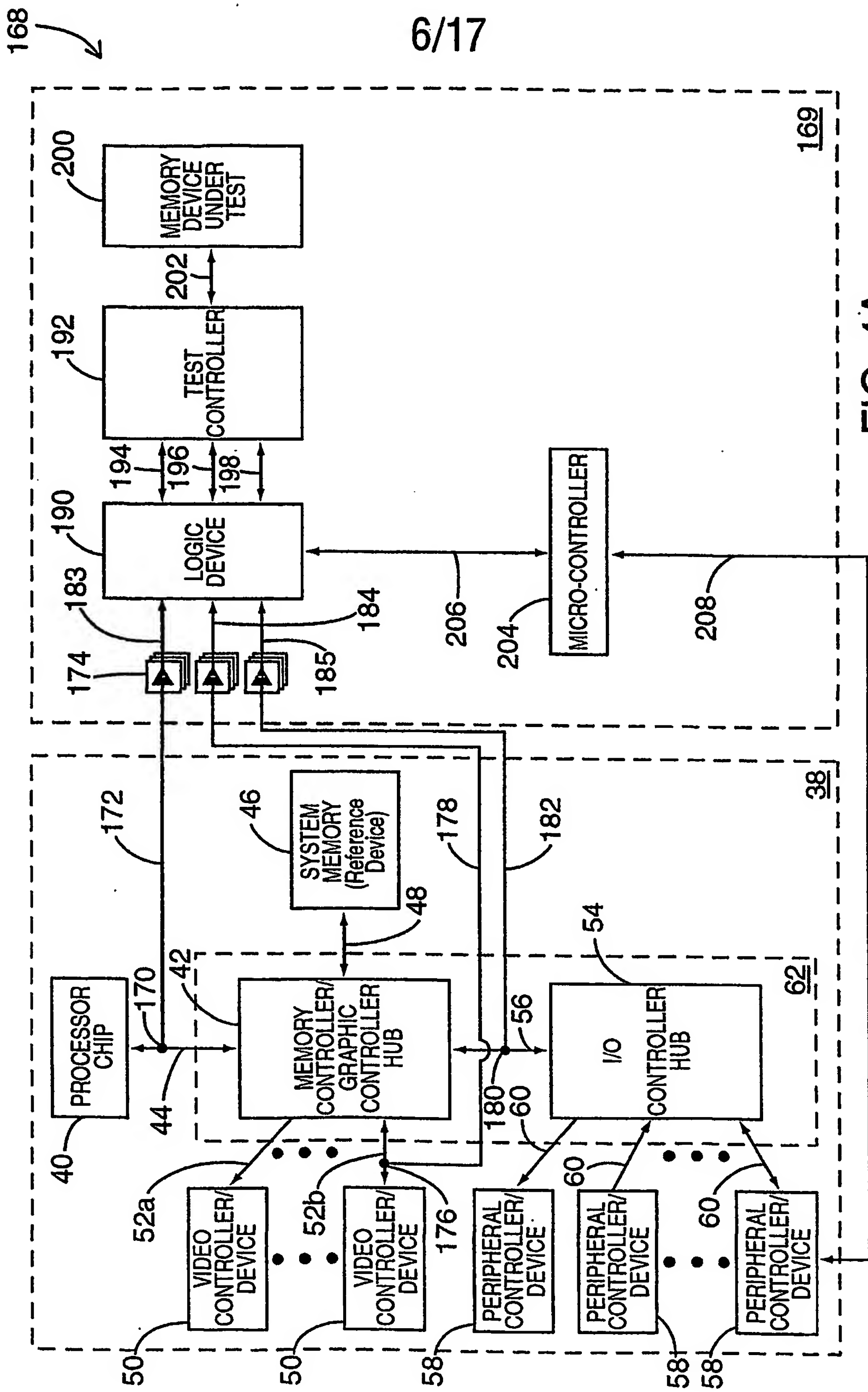

168
169
MEMORY DEVICE UNDER TEST
200
202
TEST CONTROLLER
192
194
196
198
LOGIC DEVICE
190
183
184
185
174
206
MICRO-CONTROLLER
204
208
38
SYSTEM MEMORY (Reference Device)
46
48
172
178
182
PROCESSOR CHIP
40
170
42
44
MEMORY CONTROLLER/ GRAPHIC CONTROLLER HUB
56
180
I/O CONTROLLER HUB
54
62
60
VIDEO CONTROLLER/ DEVICE
52a
52b
176
50
PERIPHERAL CONTROLLER/ DEVICE
58

FIG. 4A

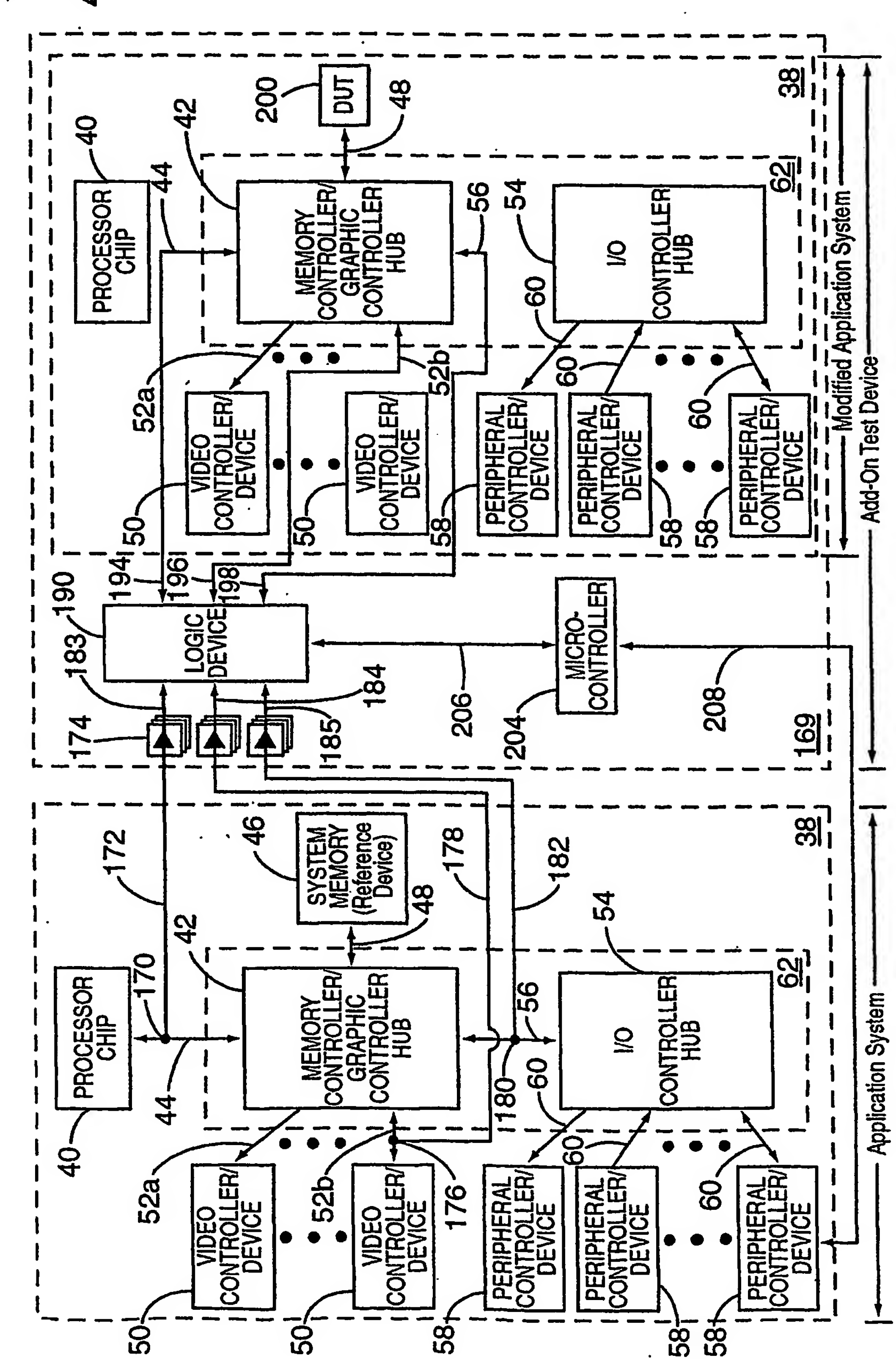

168
PROCESSOR CHIP
MEMORY CONTROLLER/ GRAPHIC CONTROLLER HUB
DUT
I/O CONTROLLER HUB
VIDEO CONTROLLER/ DEVICE
PERIPHERAL CONTROLLER/ DEVICE
LOGIC DEVICE
MICRO-CONTROLLER
SYSTEM MEMORY (Reference Device)
Modified Application System
Add-On Test Device
Application System
38
40
42
44
46
48
50
52a
52b
54
56
58
60
62
169
170
172
174
176
178
180
182
183
184
185
190
194
196
198
200
204
206
208

FIG. 4B

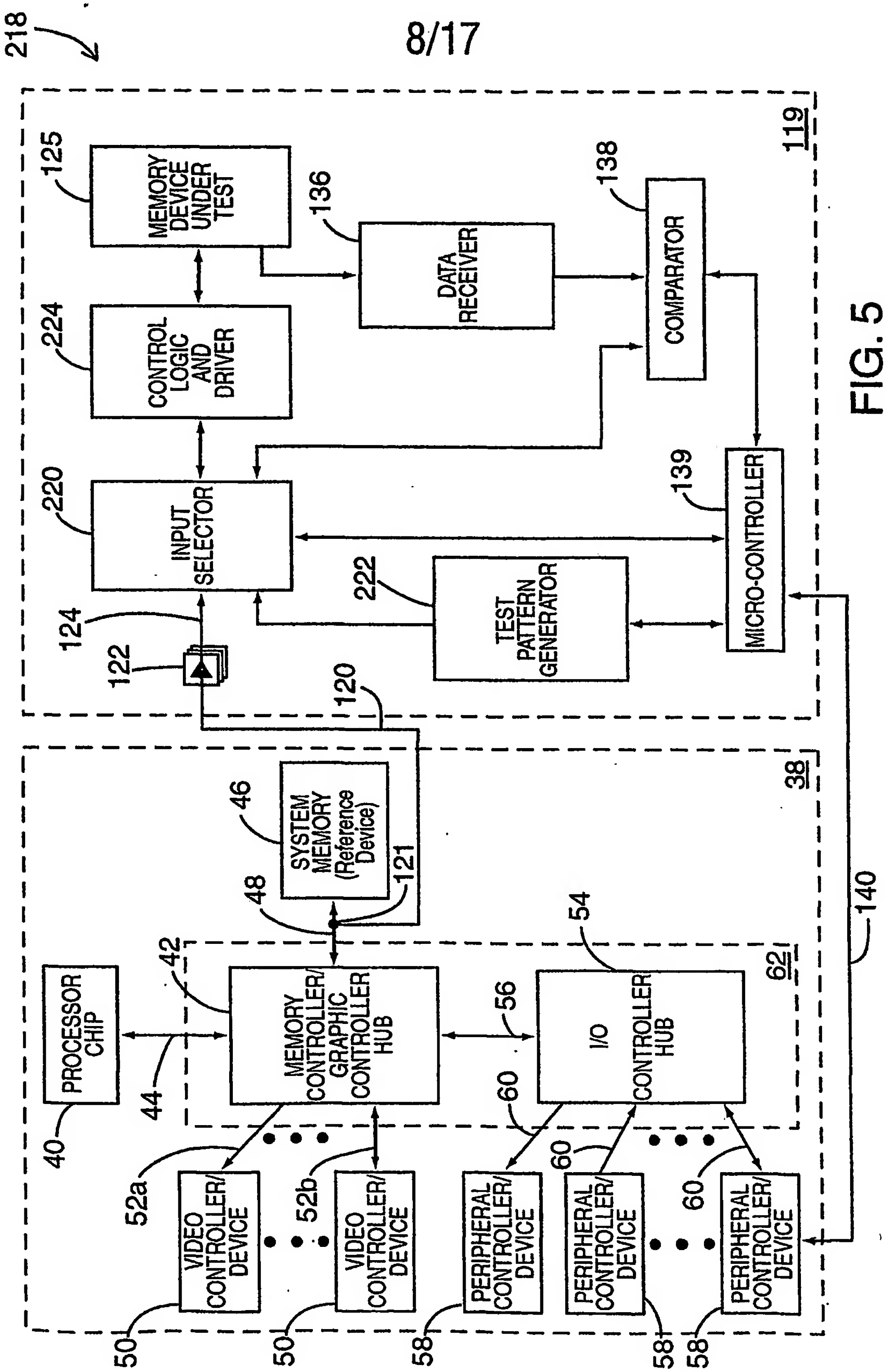
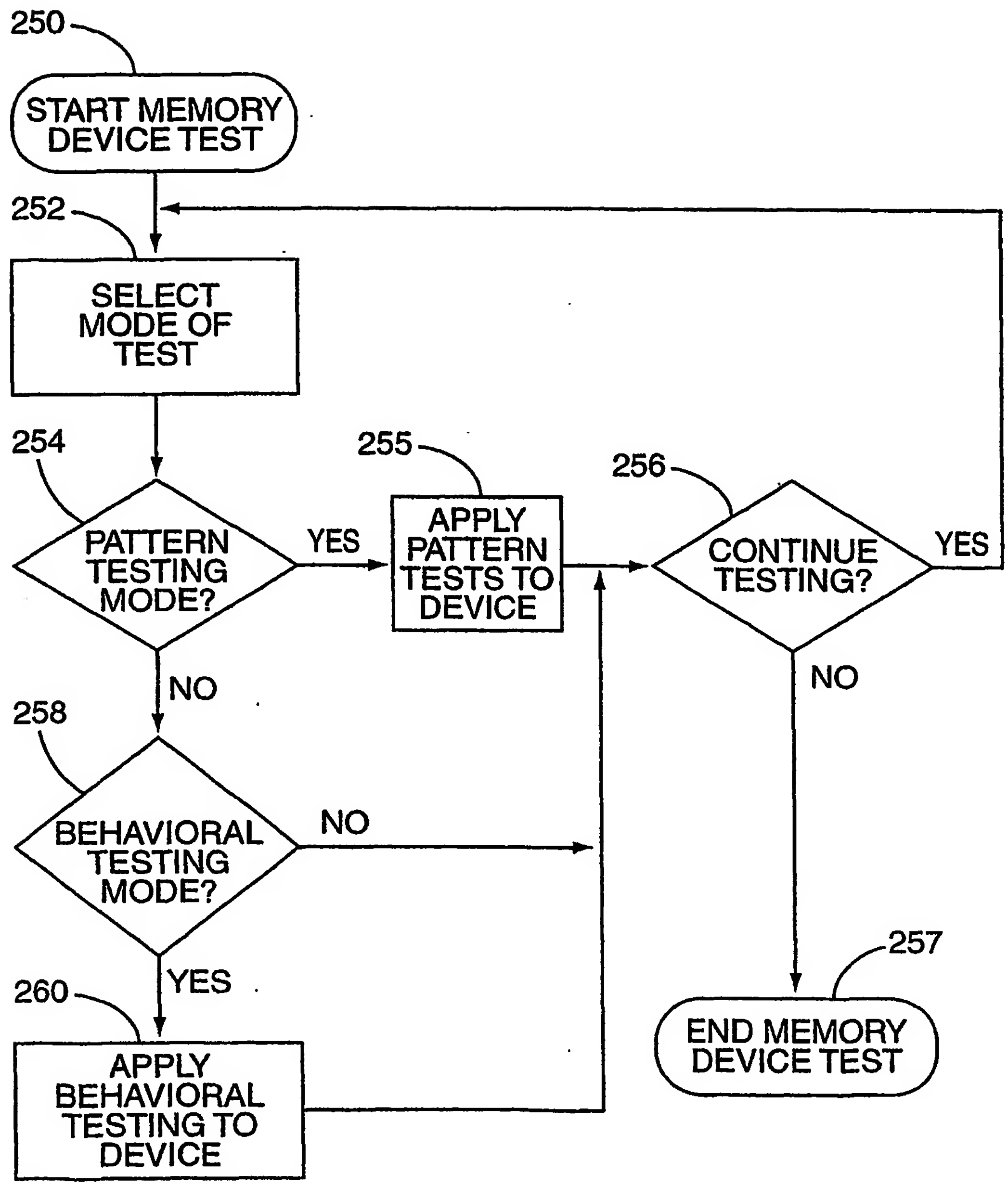

218
MEMORY DEVICE UNDER TEST
125
CONTROL LOGIC AND DRIVER
224
INPUT SELECTOR
220
124
122
DATA RECEIVER
136
COMPARATOR
138
TEST PATTERN GENERATOR
222
MICRO-CONTROLLER
139
119
120
SYSTEM MEMORY (Reference Device)
46
48
121
PROCESSOR CHIP
40
44
MEMORY CONTROLLER/ GRAPHIC CONTROLLER HUB
42
56
I/O CONTROLLER HUB
54
62
38
140
VIDEO CONTROLLER/ DEVICE
52a
52b
50
PERIPHERAL CONTROLLER/ DEVICE
60
58

FIG. 5



250
START MEMORY DEVICE TEST
252
SELECT MODE OF TEST
254
PATTERN TESTING MODE?
YES
255
APPLY PATTERN TESTS TO DEVICE
256
CONTINUE TESTING?
YES
NO
NO
258
BEHAVIORAL TESTING MODE?
NO
YES
260
APPLY BEHAVIORAL TESTING TO DEVICE
257
END MEMORY DEVICE TEST

FIG. 6

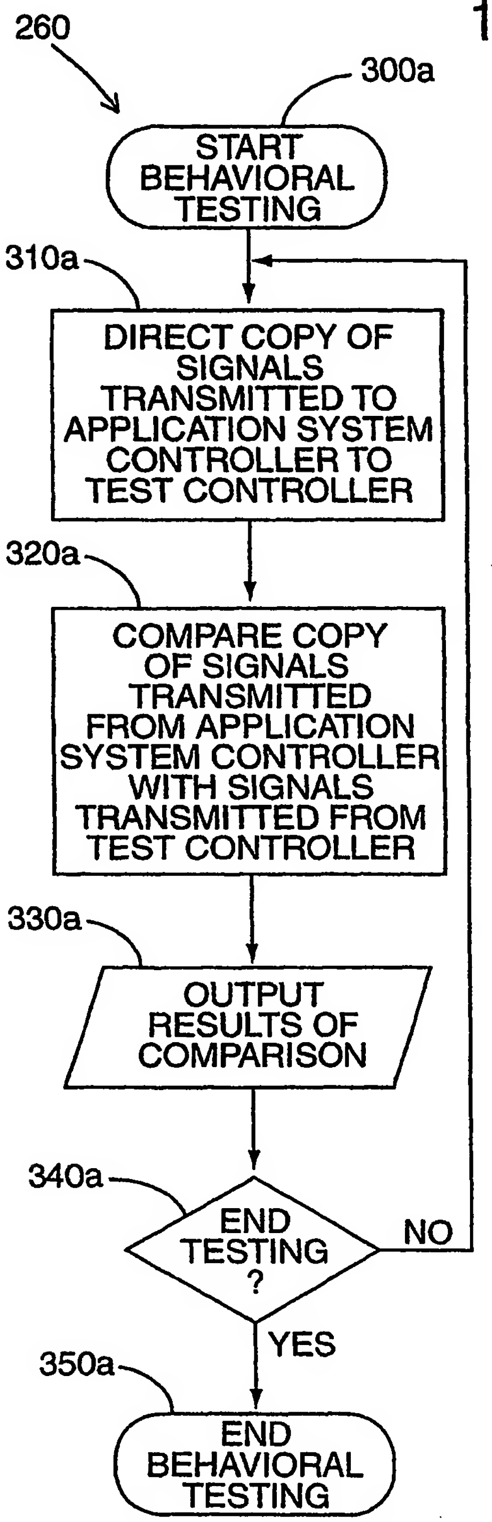

260
300a
START BEHAVIORAL TESTING
310a
DIRECT COPY OF SIGNALS TRANSMITTED TO APPLICATION SYSTEM CONTROLLER TO TEST CONTROLLER
320a
COMPARE COPY OF SIGNALS TRANSMITTED FROM APPLICATION SYSTEM CONTROLLER WITH SIGNALS TRANSMITTED FROM TEST CONTROLLER
330a
OUTPUT RESULTS OF COMPARISON
340a
END TESTING ?
NO
YES
350a
END BEHAVIORAL TESTING

FIG. 7A

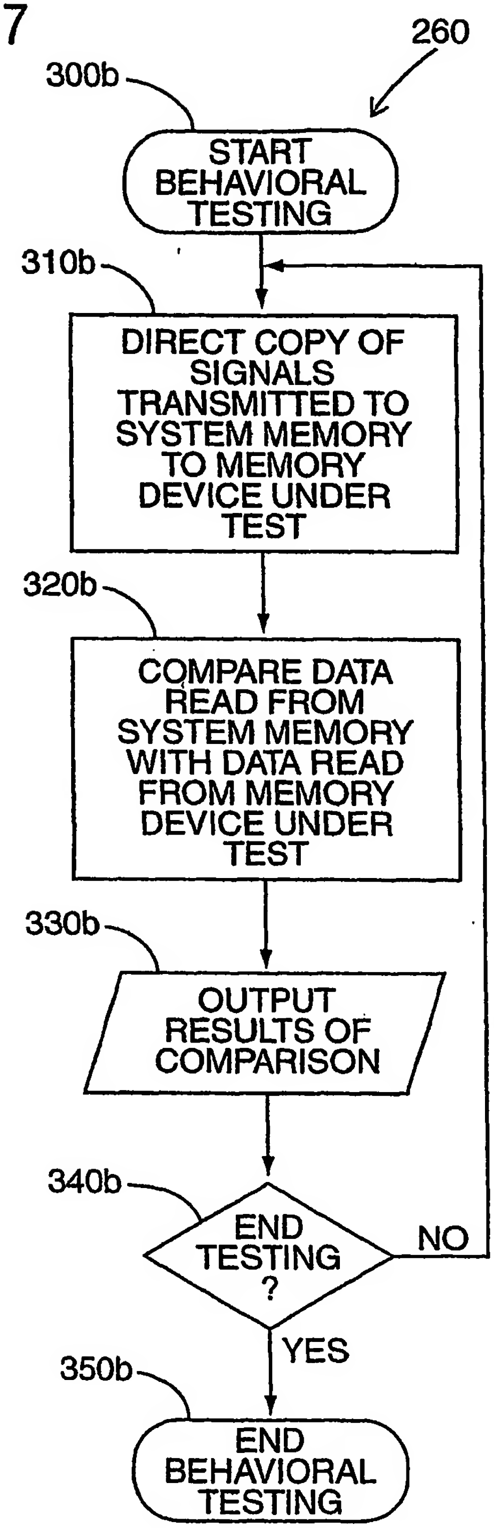

260
300b
START BEHAVIORAL TESTING
310b
DIRECT COPY OF SIGNALS TRANSMITTED TO SYSTEM MEMORY TO MEMORY DEVICE UNDER TEST
320b
COMPARE DATA READ FROM SYSTEM MEMORY WITH DATA READ FROM MEMORY DEVICE UNDER TEST
330b
OUTPUT RESULTS OF COMPARISON
340b
END TESTING ?
NO
YES
350b
END BEHAVIORAL TESTING

FIG. 7B

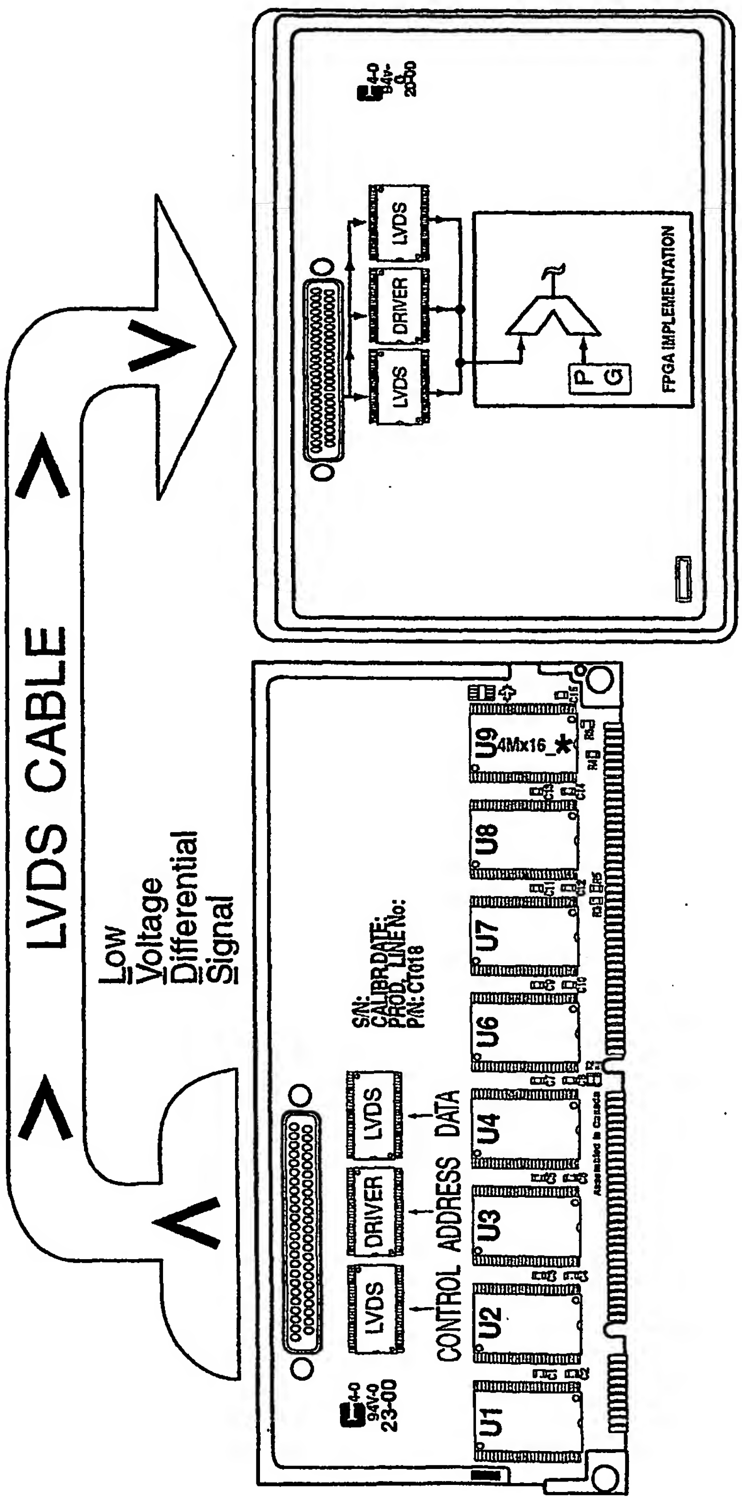

LVDS CABLE
Low
Voltage
Differential
Signal
LVDS
DRIVER
LVDS
FPGA IMPLEMENTATION
P
G
S/N:
CALIBR.DATE:
PROD. LINE No:
P/N: CT018
LVDS
DRIVER
LVDS
CONTROL ADDRESS DATA
U1
U2
U3
U4
U6
U7
U8
U9
4Mx16

FIG. 8

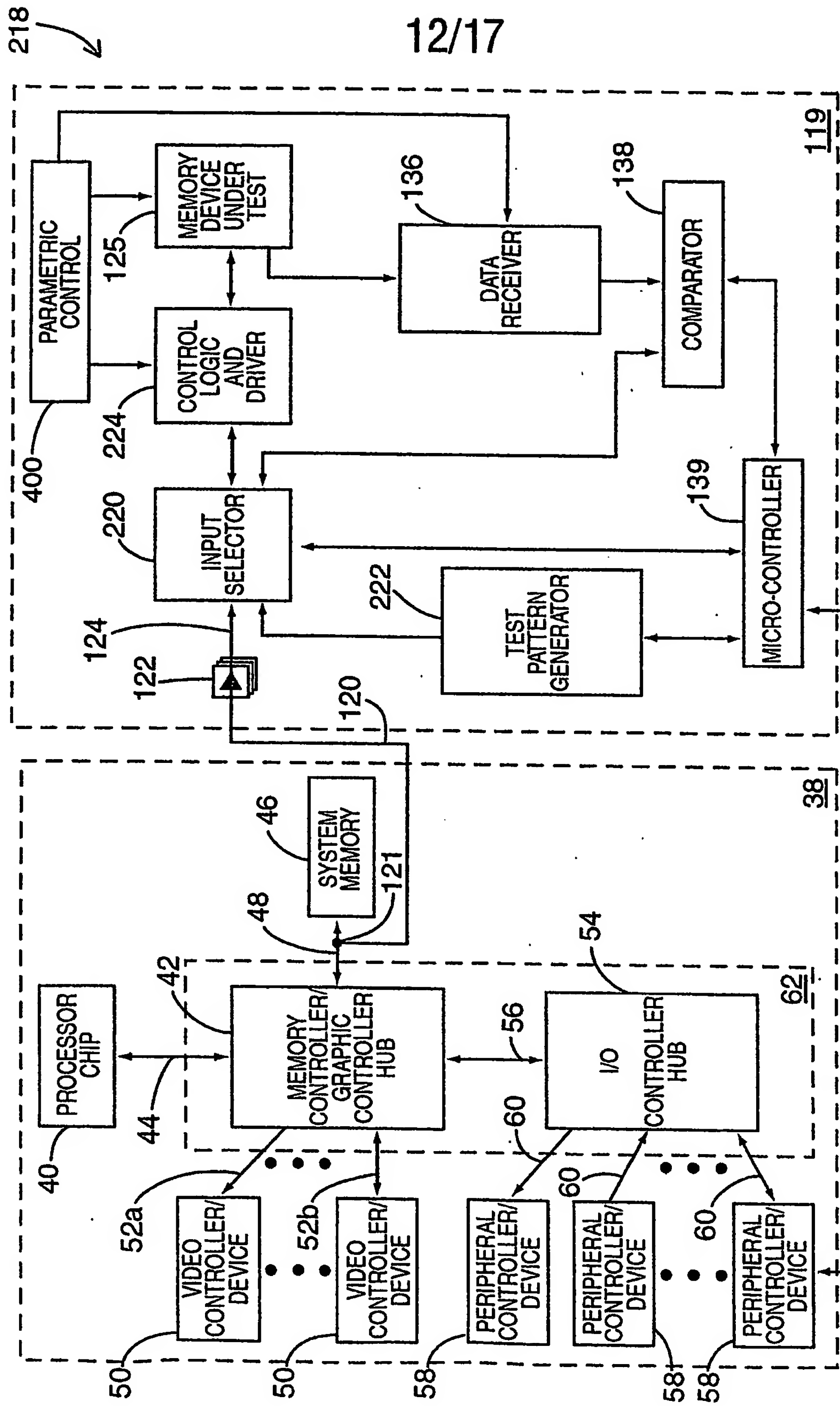

218
119
PARAMETRIC CONTROL
400
MEMORY DEVICE UNDER TEST
125
CONTROL LOGIC AND DRIVER
224
DATA RECEIVER
136
COMPARATOR
138
INPUT SELECTOR
220
TEST PATTERN GENERATOR
222
MICRO-CONTROLLER
139
124
122
120
38
SYSTEM MEMORY
46
121
48
PROCESSOR CHIP
40
MEMORY CONTROLLER/ GRAPHIC CONTROLLER HUB
42
44
56
I/O CONTROLLER HUB
54
62
140
VIDEO CONTROLLER/ DEVICE
52a
52b
50
PERIPHERAL CONTROLLER/ DEVICE
60
58

FIG. 9

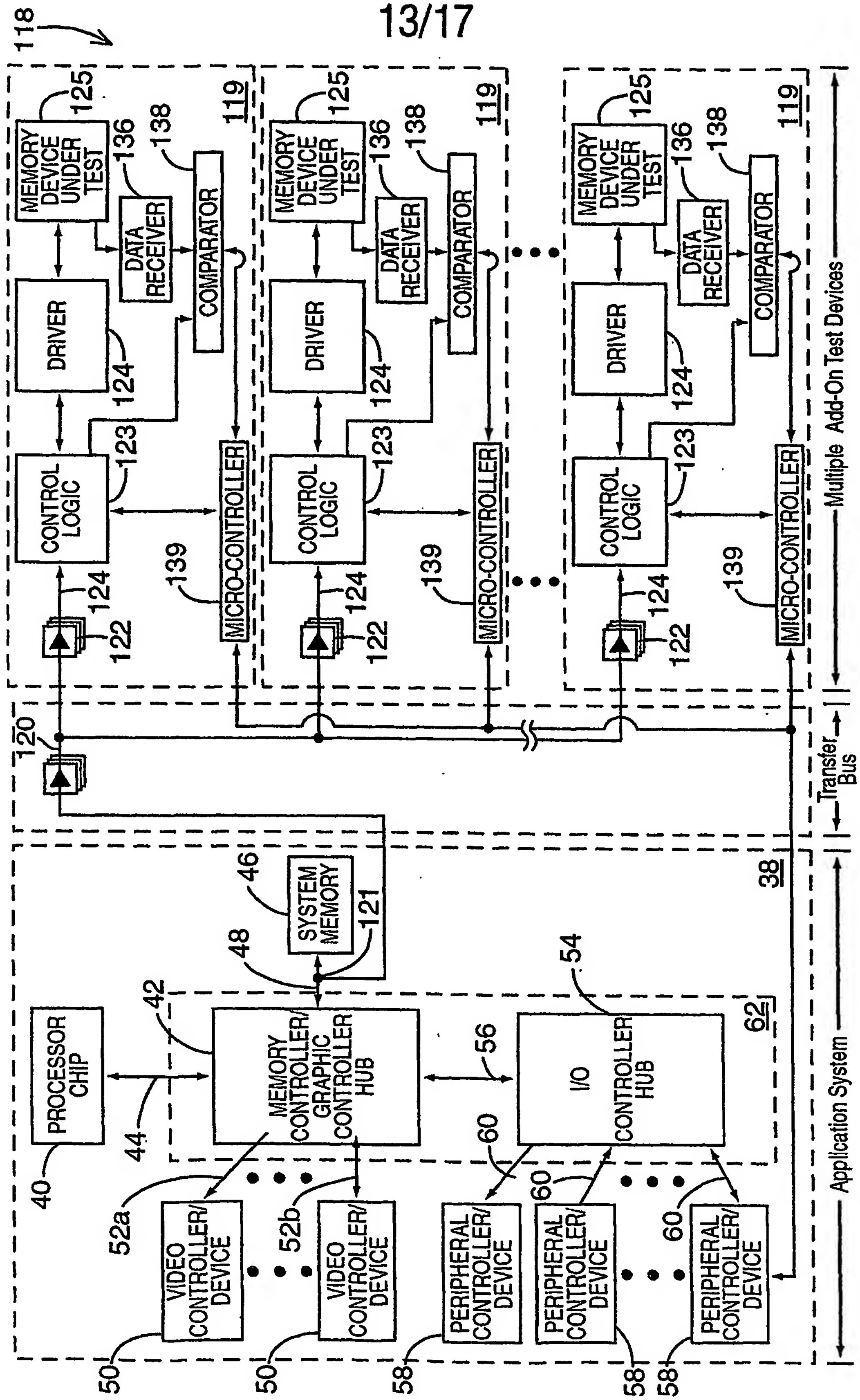

118
MEMORY DEVICE UNDER TEST
125
136
138
119
DATA RECEIVER
COMPARATOR
DRIVER
124
123
CONTROL LOGIC
MICRO-CONTROLLER
139
122
120
Multiple Add-On Test Devices
Transfer Bus
Application System
SYSTEM MEMORY
46
121
48
38
54
42
PROCESSOR CHIP
MEMORY CONTROLLER/ GRAPHIC CONTROLLER HUB
56
I/O CONTROLLER HUB
62
40
44
60
52a
52b
VIDEO CONTROLLER/ DEVICE
PERIPHERAL CONTROLLER/ DEVICE
50
58

FIG. 10

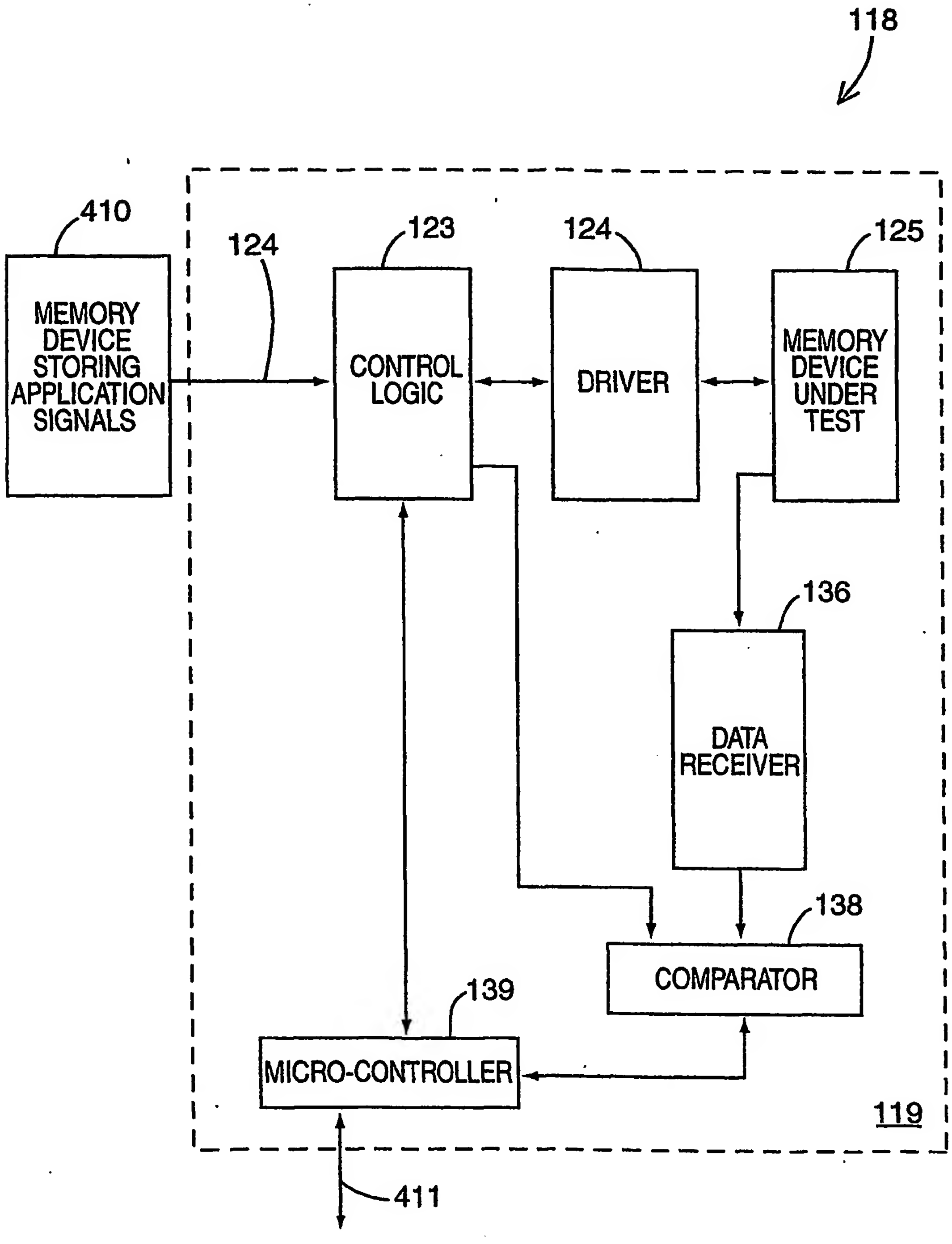

118
410
MEMORY DEVICE STORING APPLICATION SIGNALS
124
123
CONTROL LOGIC
124
DRIVER
125
MEMORY DEVICE UNDER TEST
136
DATA RECEIVER
138
COMPARATOR
139
MICRO-CONTROLLER
119
411

FIG. 11A

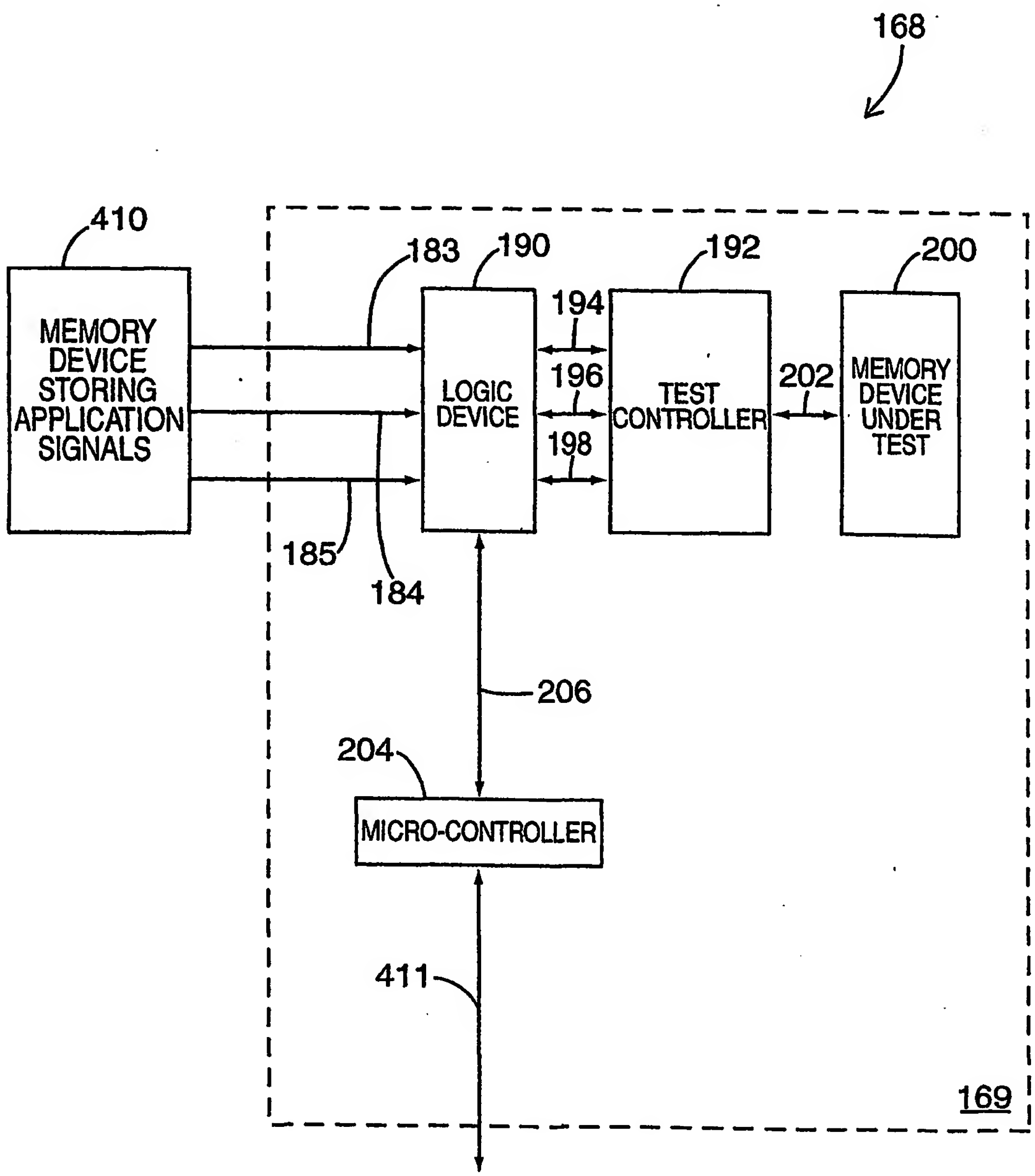
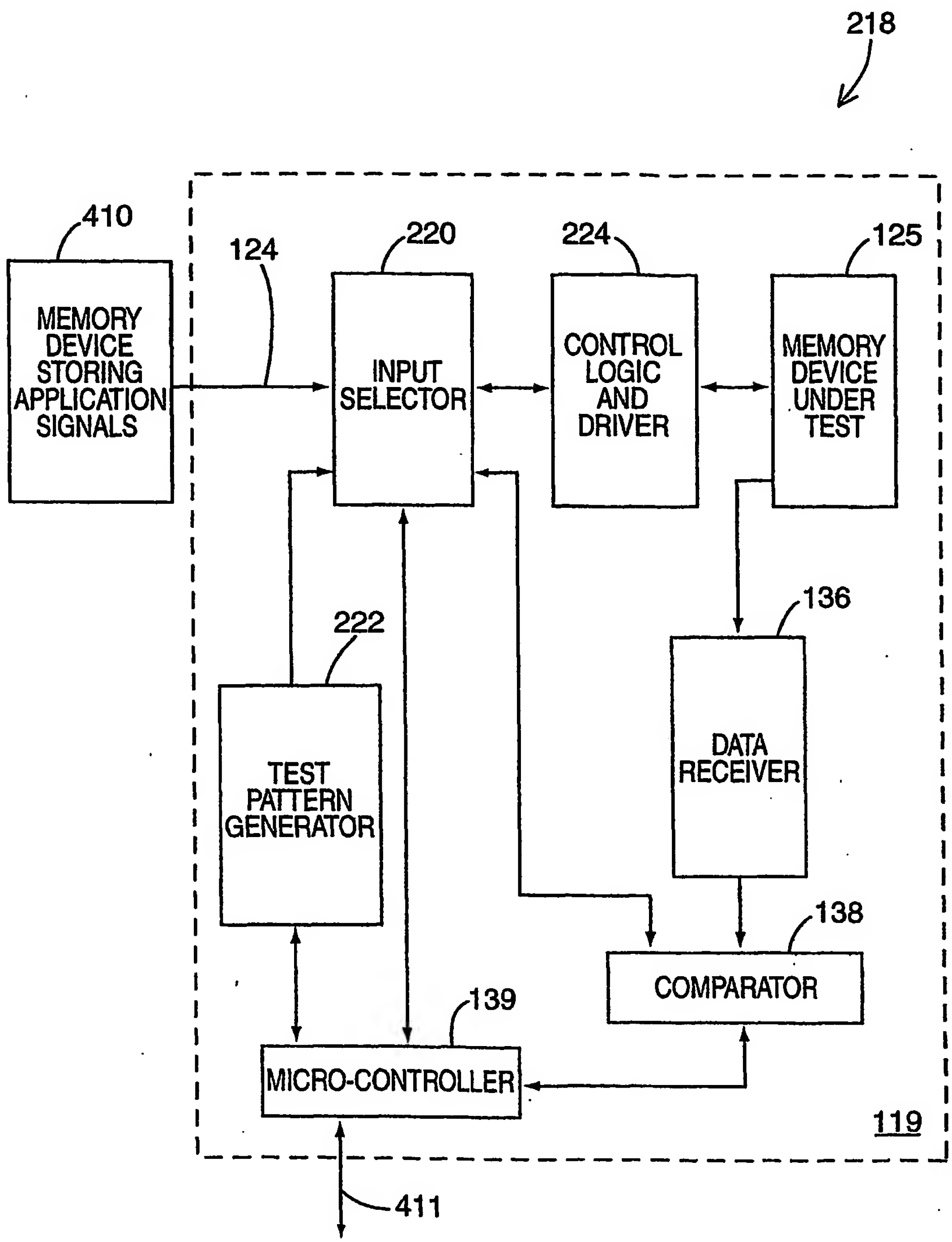

168
410
MEMORY DEVICE STORING APPLICATION SIGNALS
183
190
192
200
LOGIC DEVICE
194
196
198
TEST CONTROLLER
202
MEMORY DEVICE UNDER TEST
185
184
206
204
MICRO-CONTROLLER
411
169

FIG. 11B



218
410
MEMORY DEVICE STORING APPLICATION SIGNALS
124
220
INPUT SELECTOR
224
CONTROL LOGIC AND DRIVER
125
MEMORY DEVICE UNDER TEST
222
TEST PATTERN GENERATOR
136
DATA RECEIVER
138
COMPARATOR
139
MICRO-CONTROLLER
119
411

FIG. 11C

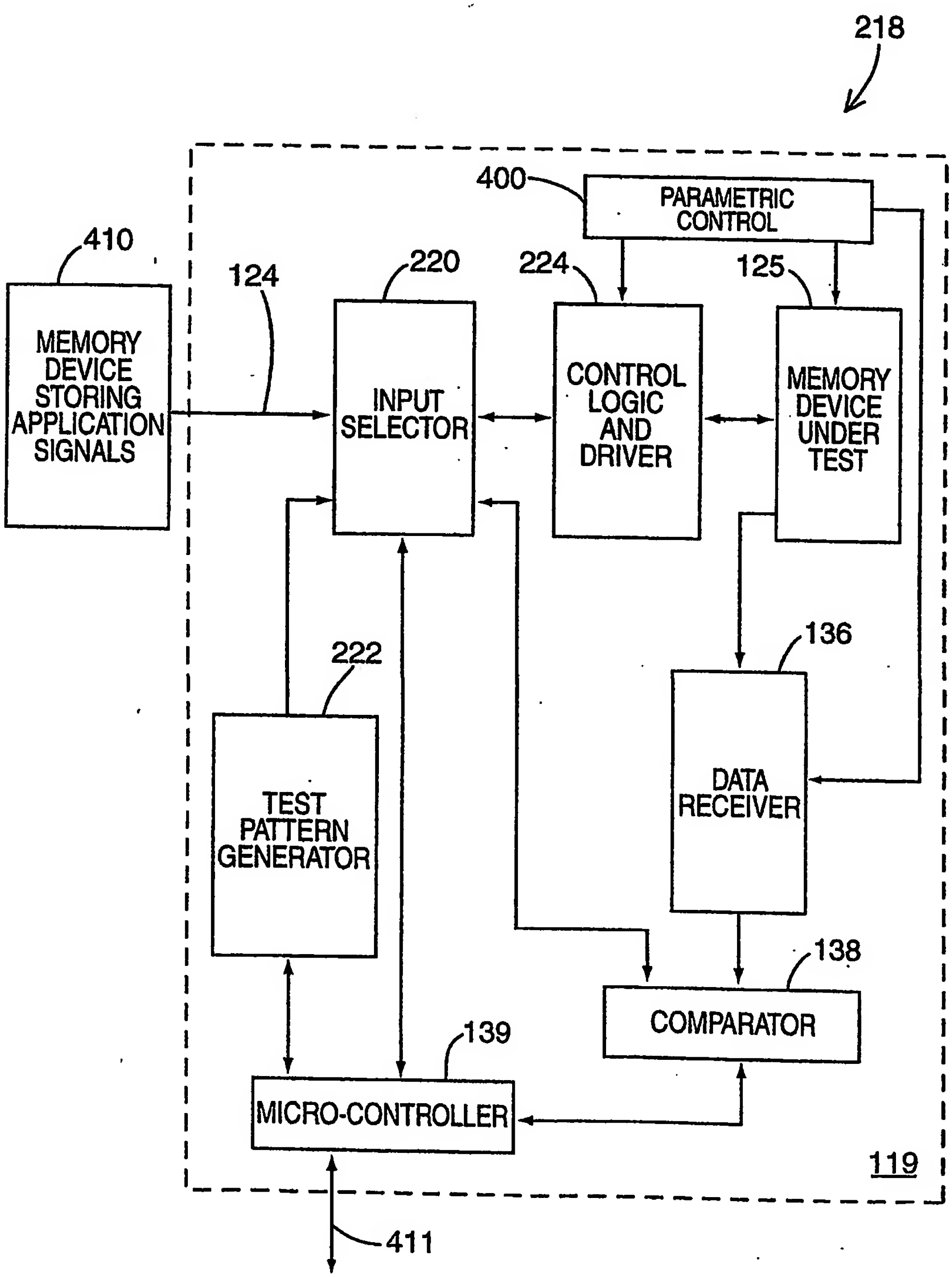

218
400
PARAMETRIC CONTROL
410
MEMORY DEVICE STORING APPLICATION SIGNALS
124
220
INPUT SELECTOR
224
CONTROL LOGIC AND DRIVER
125
MEMORY DEVICE UNDER TEST
136
DATA RECEIVER
222
TEST PATTERN GENERATOR
138
COMPARATOR
139
MICRO-CONTROLLER
119
411

FIG. 11D